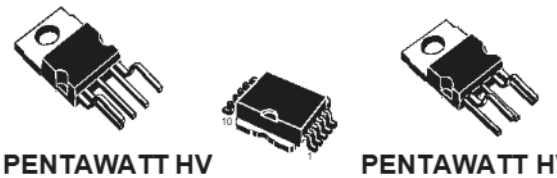
VIPer50B
VIPer50BSP

SMPS PRIMARY I.C.

TARGET DATA

TYPE	V_{DSS}	I_n	$R_{DS(on)}$
VIPer50B/BSP	400 V	3 A	2.2 Ω



PENTAWATT HV **PENTAWATT HV (022Y)**

PowerSO-10

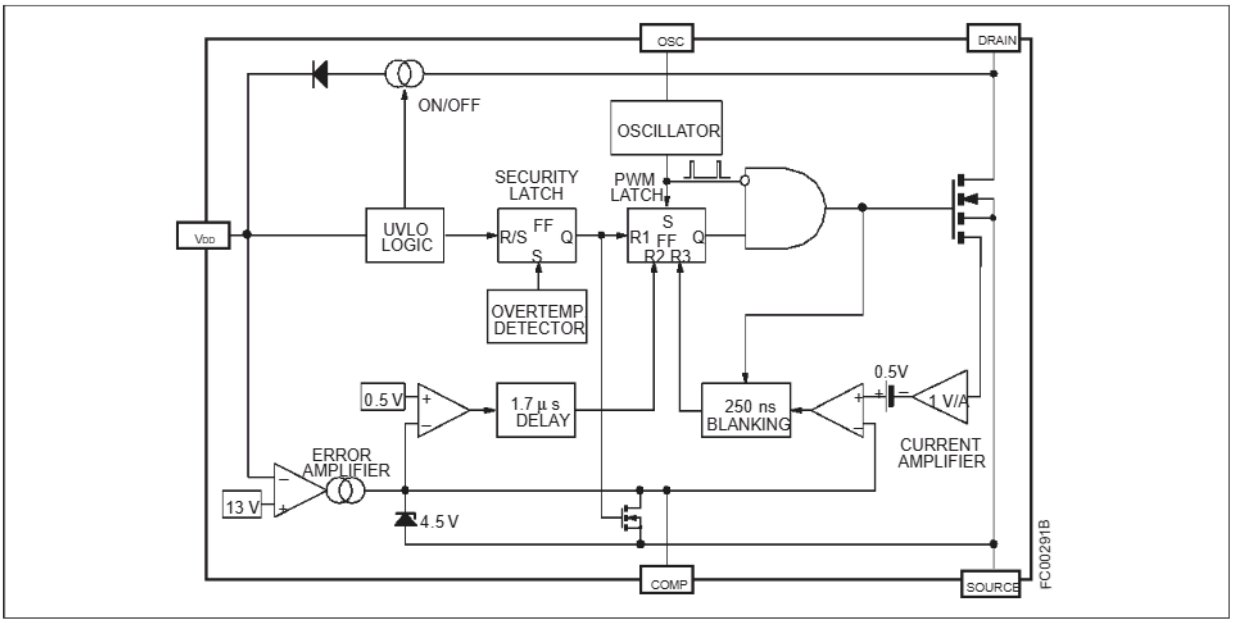
FEATURE

- ADJUSTABLE SWITCHING FREQUENCY UP TO 200KHZ
- CURRENT MODE CONTROL
- SOFT START AND SHUT DOWN CONTROL
- AUTOMATIC BURST MODE OPERATION IN STAND-BY CONDITION ABLE TO MEET "BLUE ANGEL" NORM (<1W TOTAL POWER CONSUMPTION)
- INTERNALLY TRIMMED ZENER REFERENCE
- UNDERVOLTAGE LOCK-OUT WITH HYSTERESIS
- INTEGRATED START-UP SUPPLY
- AVALANCHE RUGGED
- OVERTEMPERATURE PROTECTION
- LOW STAND-BY CURRENT
- ADJUSTABLE CURRENT LIMITATION

DESCRIPTION

VIPer50B made using VIPower M0 Technology combines on the same silicon chip a state-of-the-art PWM circuit together with an optimized high voltage avalanche rugged Vertical Power MOSFET (400 V / 3 A). Typical applications cover off line power supplies with a secondary power capability of 50W in a US mains lines configuration. It is compatible from both primary or secondary regulation loop despite using around 50% less components when compared with a discrete solution. Burst mode operation is an additional feature of this device, offering the possibility to operate in stand-by mode without extra components.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING

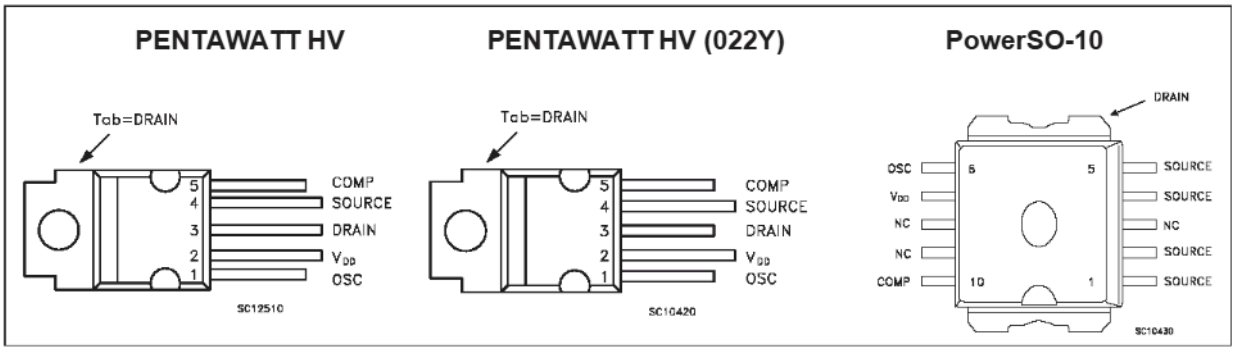
Symbol	Parameter	Value	Unit
V_{DS}	Continuous Drain-Source Voltage (Tj = 25 to 125°C)	-0.3 to 400	V
I_D	Maximum Current	Internally Limited	A
V_{DD}	Supply Voltage	0 to 15	V
V_{OSC}	Voltage Range Input	0 to V_{DD}	V
V_{COMP}	Voltage Range Input	0 to 5	V
I_{COMP}	Maximum Continuous Current	±2	mA
V_{esd}	Electrostatic discharge (R = 1.5 KΩ C = 100pF)	4000	V
$I_{D(AR)}$	Avalanche Drain-Source Current, Repetitive or Not-Repetitive (T_C = 100 °C, Pulse Width Limited by T_J max, δ <1%)	TBD	A
P_{tot}	Power Dissipation at Tc = 25°C	60	W
T_j	Junction Operating Temperature	Internally Limited	°C
T_{stg}	Storage Temperature	-65 to 150	°C

THERMAL DATA

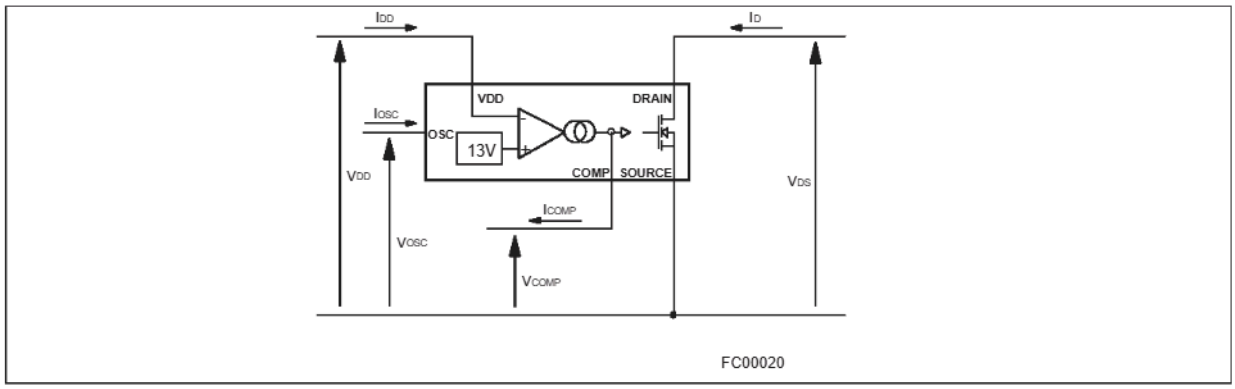
			PENTAWATT-HV	PowerSO-10(*)	
$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	1.9	1.9	°C/W
$R_{thj\text{-}amb.}$	Thermal Resistance Ambient-case	Max	60	50	°C/W

(*) When mounted using the minimum recommended pad size on FR-4 board.

CONNECTION DIAGRAMS (Top View)



CURRENT AND VOLTAGE CONVENTIONS



ORDERING NUMBERS

PENTAWATT HV	PENTAWATT HV (022Y)	PowerSO-10
VIPer50B	VIPer50B (022Y)	VIPer50BSP

PINS FUNCTIONAL DESCRIPTION

DRAIN PIN:

Integrated power MOSFET drain pin. It provides internal bias current during start-up via an integrated high voltage current source which is switched off during normal operation. The device is able to handle an unclamped current during its normal operation, assuring self protection against voltage surges, PCB stray inductance, and allowing a snubberless operation for low output power.

SOURCE PIN:

Power MOSFET source pin. Primary side circuit common ground connection.

VDD PIN :

This pin provides two functions :

- It corresponds to the low voltage supply of the control part of the circuit. If V_{DD} goes below 8V, the start-up current source is activated and the output power MOSFET is switched off until the V_{DD} voltage reaches 11V. During this phase, the internal current consumption is reduced, the V_{DD} pin is sourcing a current of about 2mA and the COMP pin is shorted to ground. After that, the current source is shut down, and the device tries to start up by switching again.
- This pin is also connected to the error amplifier, in order to allow primary as well as secondary regulation configurations. In case of primary regulation, an internal 13V trimmed reference voltage is used to maintain V_{DD} at 13V. For secondary regulation, a voltage between 8.5V and 12.5V will be put on V_{DD} pin by transformer design, in order to stuck the output of the transconductance amplifier to the high state. The COMP pin behaves as a constant current source, and can easily be connected to the output of an optocoupler. Note that any overvoltage due to regulation loop failure is still detected by the error amplifier through the V_{DD} voltage, which cannot overpass 13V. The output voltage will be somewhat higher than the nominal one, but still under control.

COMP PIN :

This pin provides two functions :

- It is the output of the error transconductance amplifier, and allows for the connection of a compensation network to provide the desired transfer function of the regulation loop. Its bandwidth can be easily adjusted to the needed value with usual components value. As stated above, secondary regulation configurations are also implemented through the COMP pin.
- When the COMP voltage is going below 0.5V, the shut-down of the circuit occurs, with a zero duty cycle for the power MOSFET. This feature can be used to switch off the converter, and is automatically activated by the regulation loop (whatever is the configuration) to provide a burst mode operation in case of negligible output power or open load condition.

OSC PIN :

An R_T-C_T network must be connected on that pin to define the switching frequency. Note that despite the connection of R_T to V_{DD}, no significant frequency change occurs for V_{DD} varying from 8V to 15V. It provides also a synchronisation capability, when connected to an external frequency source.

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
$I_{D(ar)}$	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max, $\delta < 1\%$) (see fig. 12)	TBD	A
$E_{(ar)}$	Single Pulse Avalanche Energy (starting T_j = 25 °C, $I_D = I_{D(ar)}$) (see fig. 12)	TBD	mJ

ELECTRICAL CHARACTERISTICS (T_J = 25 °C, V_{DD} = 13 V, unless otherwise specified)

POWER SECTION

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Voltage	I_D = 1 mA V_{COMP} = 0 V (see fig. 5)	400			V
I_{DSS}	Off-State Drain Current	V_{COMP} = 0 V T_J= 125 °C V_{DS} = 400 V			1	mA
$R_{DS(on)}$	Static Drain Source on Resistance	I_D = 2 A I_D = 2 A T_J= 100 °C		1.8	2.2 4.0	Ω Ω
t_f	Fall Time	I_D = 0.2 A V_{in} = 300 V (1) (see fig. 3)		100		ns
t_r	Rise Time	I_D = 2 A V_{in} = 300 V (1) (see fig. 3)		50		ns
C_{OSS}	Output Capacitance	V_{DS} = 25 V		150		pF

(1) On Inductive Load, Clamped.

SUPPLY SECTION

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{DDch}	Start-up Charging Current	V_{DD} = 5 V V_{DS} = 70 V (see fig. 2 and fig.15)		-2		mA
I_{DD0}	Operating Supply Current	V_{DD} = 12 V, F_{SW} = 0 KHz (see fig. 2)		12	16	mA
I_{DD1}	Operating Supply Current	V_{DD} = 12 V, F_{SW} = 100 KHz		14		mA
I_{DD2}	Operating Supply Current	V_{DD} = 12 V, F_{SW} = 200 KHz		16		mA
V_{DDoff}	Undervoltage Shutdown	(see fig. 2)		8		V
V_{DDon}	Undervoltage Reset	(see fig. 2)		11	12	V
V_{DDhyst}	Hysteresis Start-up	(see fig. 2)	2.4	3		V

ELECTRICAL CHARACTERISTICS (continued)

OSCILLATOR SECTION

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
F_{SW}	Oscillator Frequency Total Variation	R_T = 8.2 KΩ C_T =2.4 nF V_{DD} = 9 to15 V with R_T ± 1% C_T ± 5% (see fig.6 and fig.9)	90	100	110	KHz
V_{OSCih}	Oscillator Peak Voltage			7.1		V
V_{OSCil}	Oscillator Valley Voltage			3.7		V

ERROR AMPLIFIER SECTION

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DDreg}	VDD Regulation Point	I_{COMP} = 0 mA (see fig.1)	12.6	13	13.4	V
ΔV_{DDreg}	Total Variation	T_J = 0 to 100 °C		2		%
G_{BW}	Unity Gain Bandwidth	From Input = V_{DD} to Output = V_{COMP} COMP pin is open (see fig. 10)		150		KHz
A_{VOL}	Open Loop Voltage Gain	COMP pin is open (see fig. 10)	45	52		dB
G_m	DC Transconductance	V_{COMP} = 2.5 V (see fig. 1)	1.1	1.5	1.9	mA/V
V_{COMPLO}	Output Low Level	I_{COMP} = -400 µA V_{DD} = 14 V		0.2		V
V_{COMPHI}	Output High Level	I_{COMP} = 400 µA V_{DD} = 12 V		4.5		V
I_{COMPLO}	Output Low Current Capability	V_{COMP} = 2.5 V V_{DD} = 14 V		-600		µA
I_{COMPHI}	Output High Current Capability	V_{COMP} = 2.5 V V_{DD} = 12 V		600		µA

PWM COMPARATOR SECTION

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
H_{ID}	$\Delta V_{COMP}/\Delta I_{Dpeak}$	V_{COMP} = 1 to 3 V	0.7	1	1.3	V/A
$V_{COMPoff}$	V_{COMP} offset	I_{Dpeak} = 10 mA		0.5		V
I_{Dpeak}	Peak Current Limitation	V_{DD} = 12 V COMP pin open	3	4	5.4	A
t_d	Current Sense Delay to turn-off	I_D = 0.5 A		250		ns
t_b	Blanking Time			250	360	ns
$t_{on(min)}$	Minimum on Time			350		ns

SHUTDOWN AND OVERTEMPERATURE SECTION

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{COMPth}	Restart threshold	(see fig. 4)		0.5		V
t_{DISsu}	Disable Set Up Time	(see fig. 4)		1.7	5	µs
T_{tsd}	Thermal Shutdown Temperature	(see fig. 8)	140	170		°C
T_{hyst}	Thermal Shutdown Hysteresis	(see fig. 8)		40		°C

Figure 1: V_{DD} Regulation Point

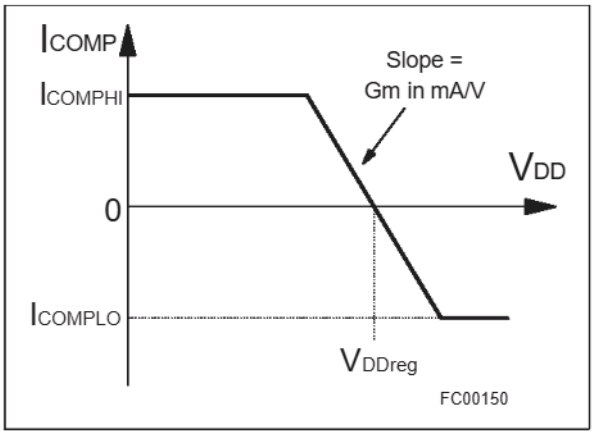


Figure 2: Undervoltage Lockout

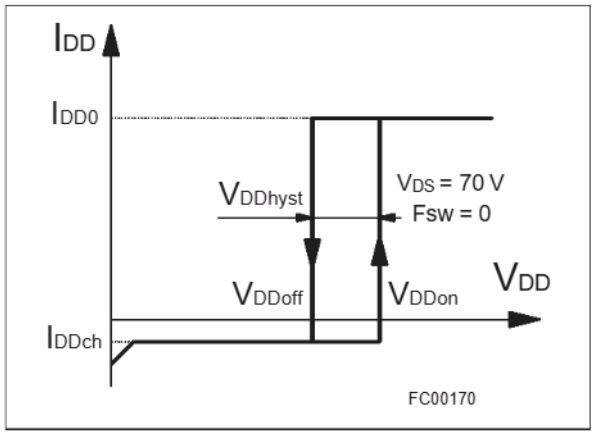


Figure 3: Transition Time

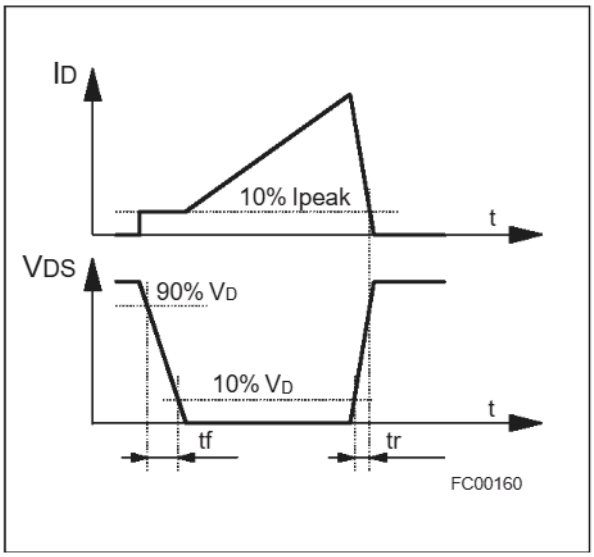


Figure 4: Shut Down Action

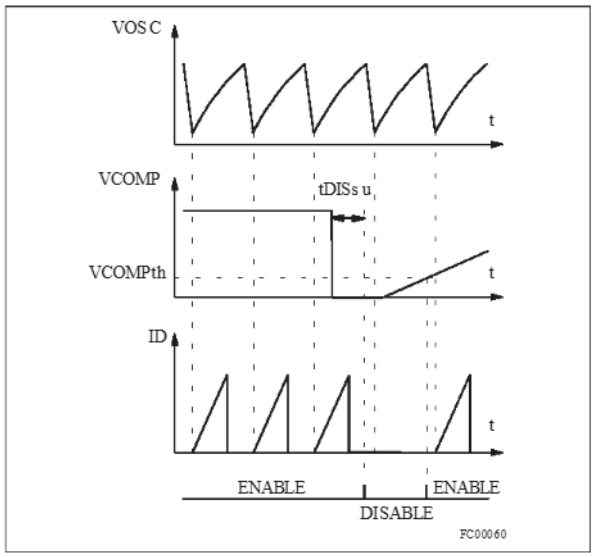


Figure 5: Breakdown Voltage vs Temperature

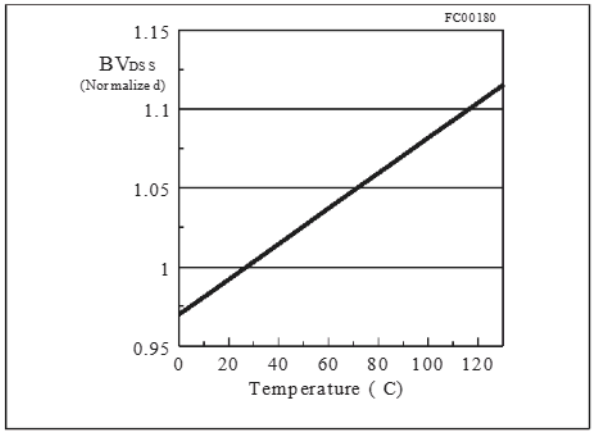


Figure 6: Typical Frequency Variation

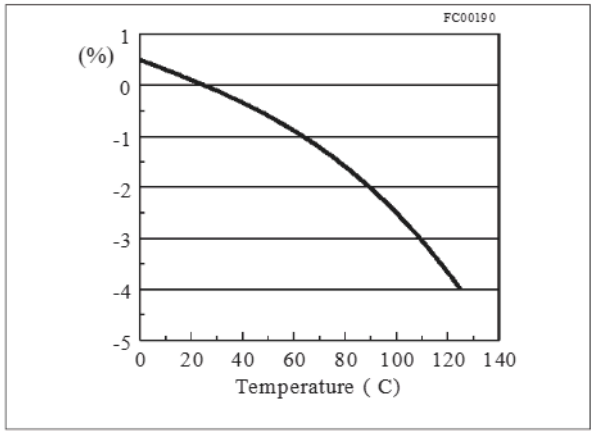


Figure 7: Start-up Waveforms

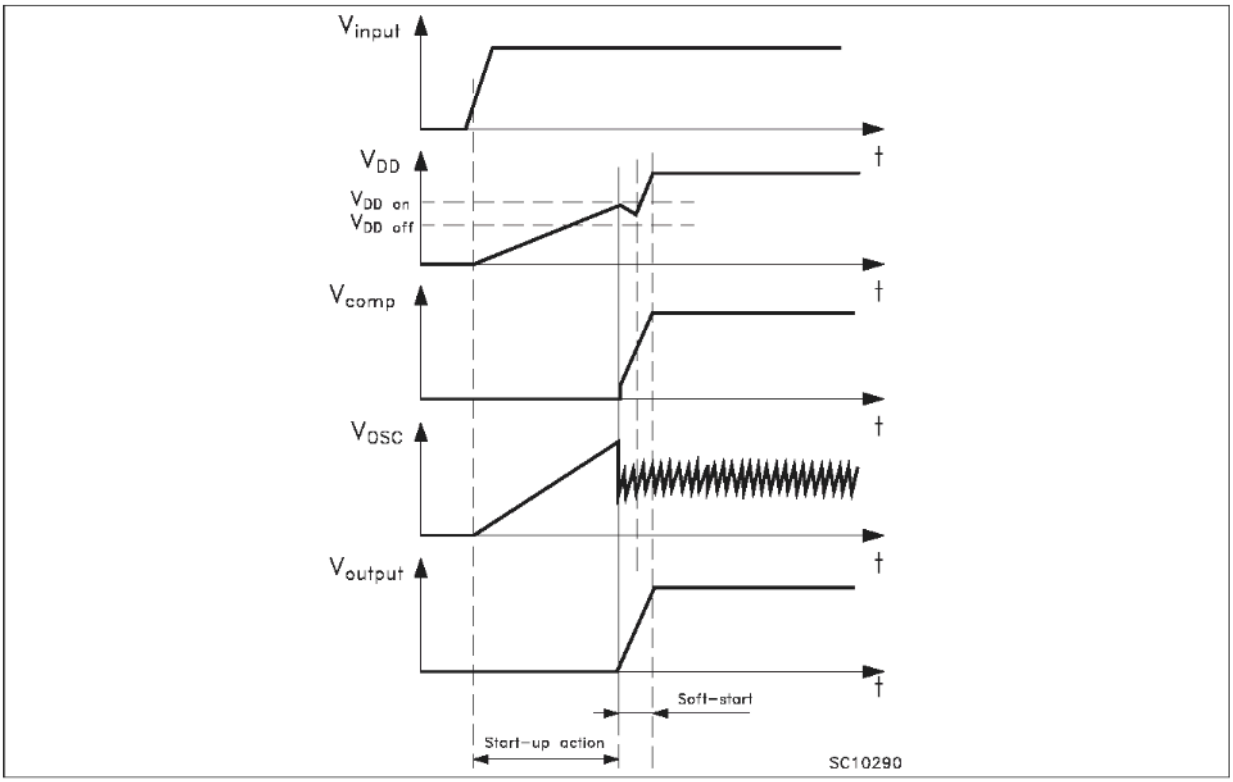


Figure 8: Overtemperature Protection

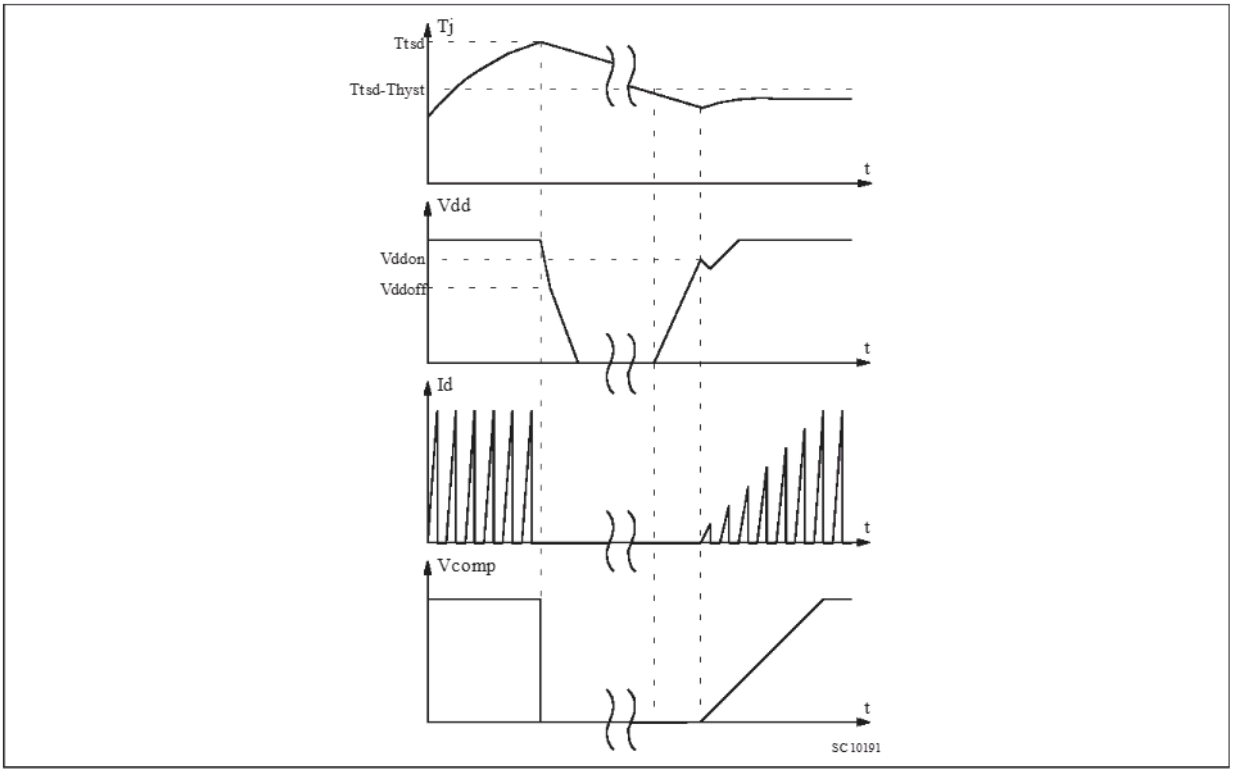
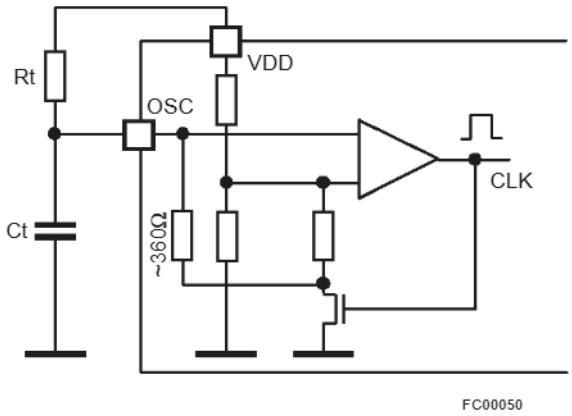


Figure 9: Oscillator

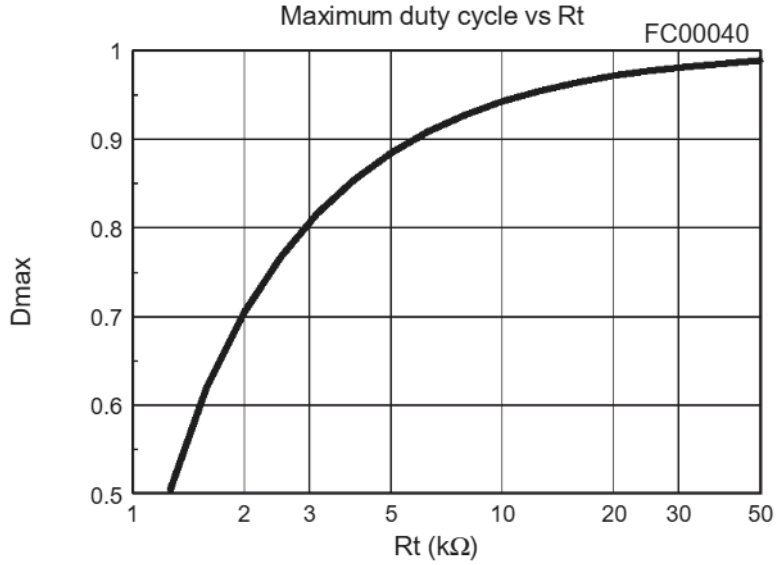


For R_T > 1.2 KΩ:

$$F_{SW} = \frac{2.3}{R_T C_T} D_{MAX}$$

$$D_{MAX} = 1 - \frac{550}{R_T - 150}$$

Recommended D_{MAX} values:
100KHz: > 80%
200KHz: > 70%



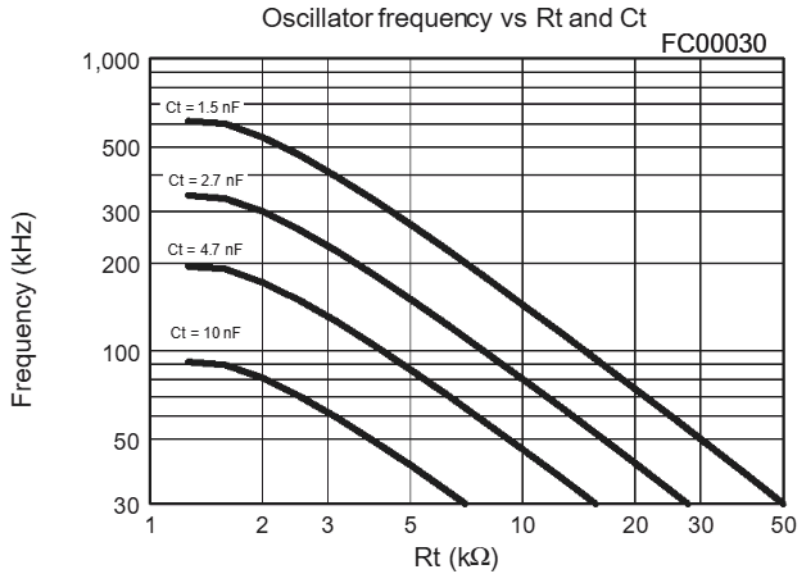


Figure 10: Error Amplifier Frequency Response

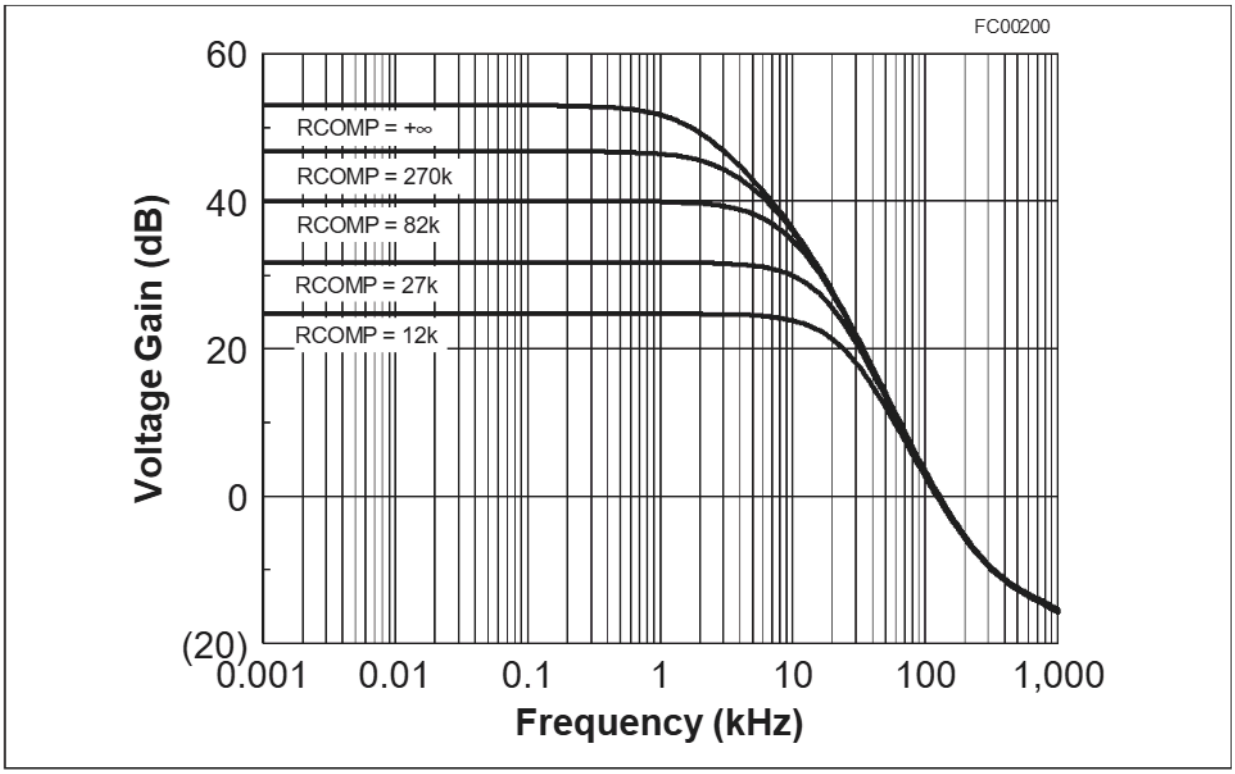


Figure 11: Error Amplifier Phase Response

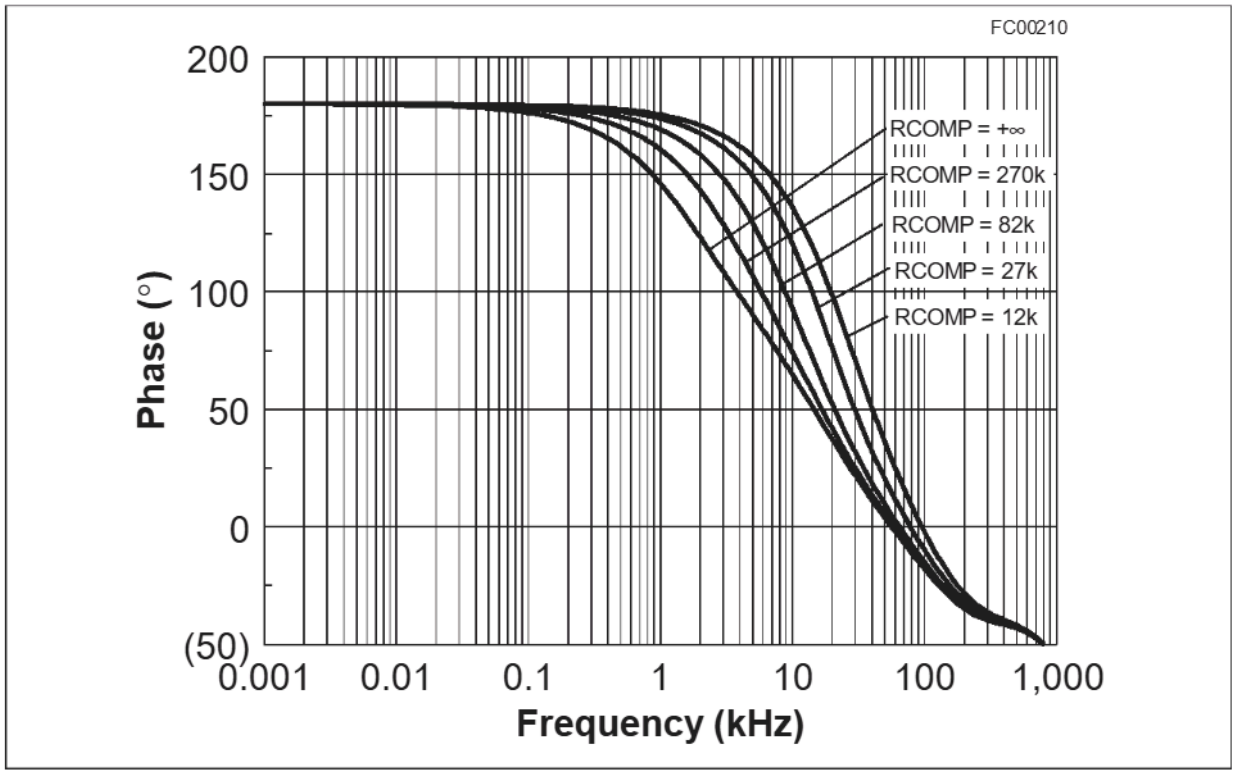


Figure 12: Avalanche Test Circuit

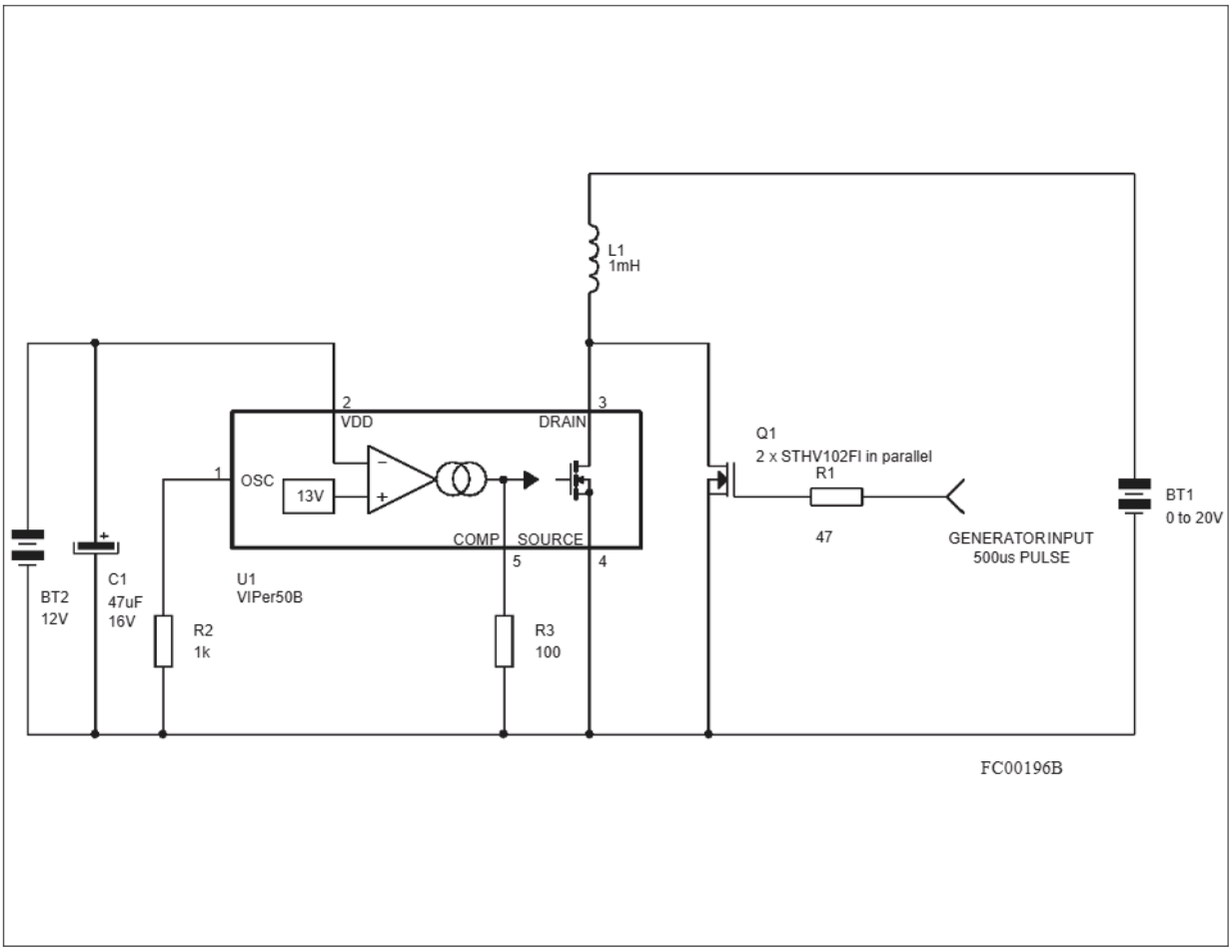


Figure 13: Off Line Power Supply With Auxiliary Supply Feedback

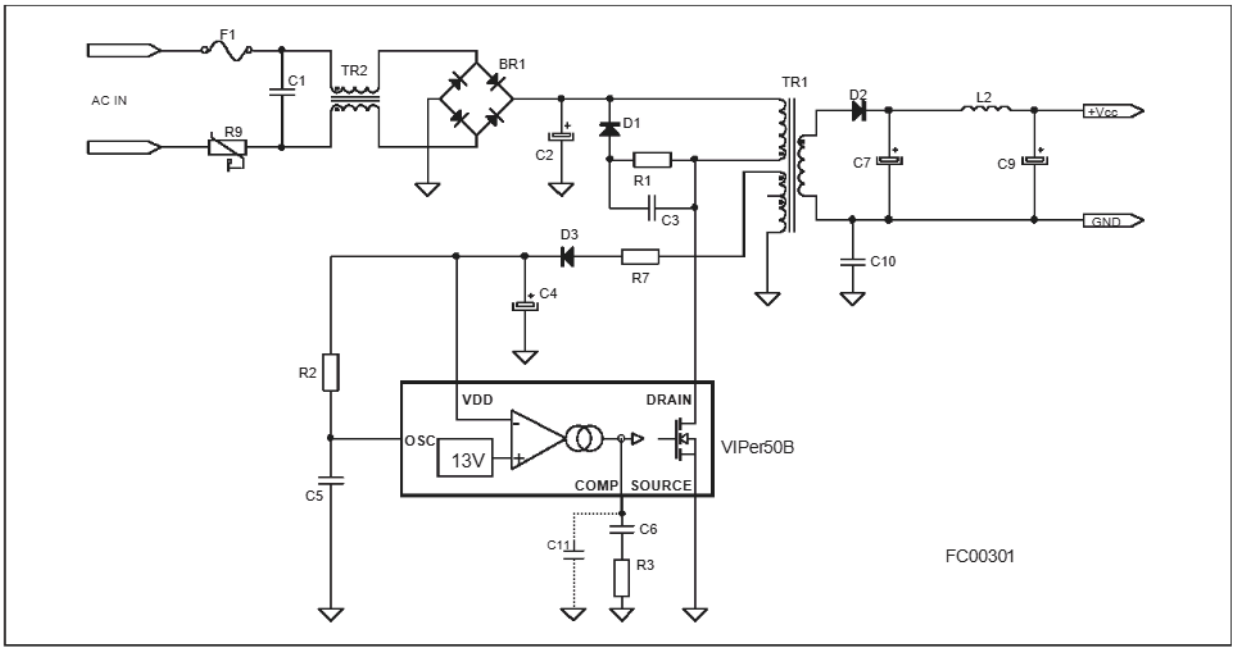
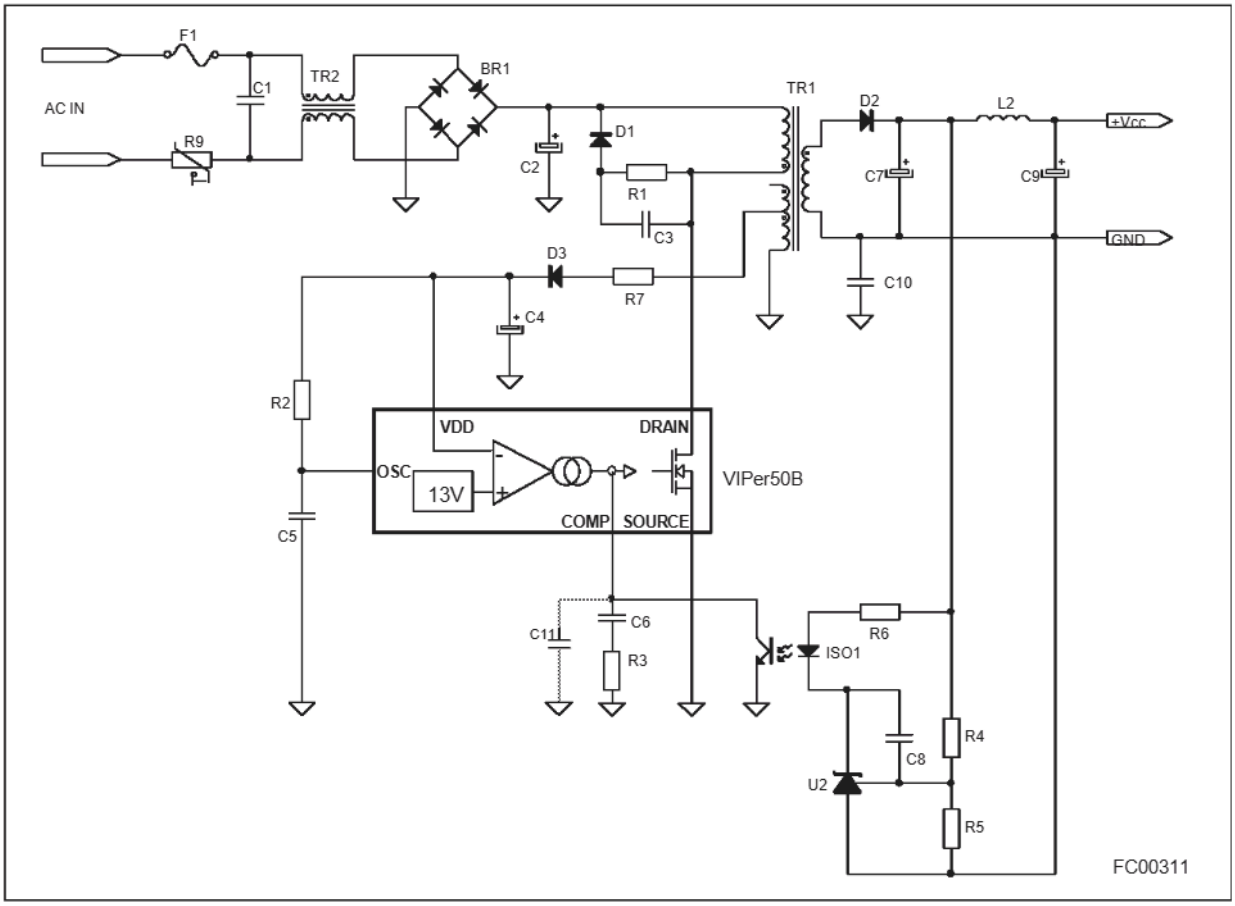


Figure 14: Off Line Power Supply With Optocoupler Feedback



OPERATION DESCRIPTION :

CURRENT MODE TOPOLOGY:

The current mode control method, like the one integrated in the VIPer50B/BSP uses two control loops - an inner current control loop and an outer loop for voltage control. When the Power MOSFET output transistor is on, the inductor current (primary side of the transformer) is monitored with a SenseFET technique and converted into a voltage V_S proportional to this current. When V_S reaches V_{COMP} (the amplified output voltage error) the power switch is switched off. Thus, the outer voltage control loop defines the level at which the inner loop regulates peak current through the power switch and the primary winding of the transformer.

Excellent open loop D.C. and dynamic line regulation is ensured due to the inherent input voltage feedforward characteristic of the current mode control. This results in an improved line regulation, instantaneous correction to line changes and better stability for the voltage regulation loop.

Current mode topology also ensures good limitation in the case of short circuit. During a first phase the output current increases slowly following the dynamic of the regulation loop. Then it reaches the maximum limitation current internally set and finally stops because the power supply on V_{DD} is no longer correct. For specific applications the maximum peak current internally set can be overridden by externally limiting the voltage excursion on the COMP pin. An integrated blanking filter inhibits the PWM comparator output for a short time after the integrated Power MOSFET is switched on. This function prevents anomalous or premature termination of the switching pulse in the case of current spikes caused by primary side capacitance or secondary side rectifier reverse recovery time.

STAND-BY MODE

Stand-by operation in nearly open load condition automatically leads to a burst mode operation allowing voltage regulation on the secondary side. The transition from normal operation to burst mode operation happens for a power P_{STBY} given by :

$$P_{STBY} = \frac{1}{2} L_P I_{STBY}^2 F_{SW}$$

Where:

L_P is the primary inductance of the transformer.

F_{SW} is the normal switching frequency.

I_{STBY} is the minimum controllable current, corresponding to the minimum on time that the device is able to provide in normal operation. This current can be computed as :

$$I_{STBY} = \frac{(t_b + t_d)\, V_{IN}}{L_P}$$

$t_b + t_d$ is the sum of the blanking time and of the propagation time of the internal current sense and comparator, and represents roughly the minimum on time of the device. Note that P_{STBY} may be affected by the efficiency of the converter at low load, and must include the power drawn on the primary auxiliary voltage.

As soon as the power goes below this limit, the auxiliary secondary voltage starts to increase above the 13V regulation level forcing the output voltage of the transconductance amplifier to low state ($V_{COMP} < V_{COMPth}$). This situation leads to the shutdown mode where the power switch is maintained in the off state, resulting in missing cycles and zero duty cycle. As soon as V_{DD} gets back to the regulation level and the V_{COMPth} threshold is reached, the device operates again. The above cycle repeats indefinitely, providing a burst mode of which the effective duty cycle is much lower than the minimum one when in normal operation. The equivalent switching frequency is also lower than the normal one, leading to a reduced consumption on the input mains lines. This mode of operation allows the VIPer50B/BSP to meet the new German "Blue Angel" Norm with less than 1W total power consumption for the system when working in stand-by. The output voltage remains regulated around the normal level, with a low frequency ripple corresponding to the burst mode. The amplitude of this ripple is low, because of the output capacitors and of the low output current drawn in such conditions.The normal operation resumes automatically when the power get back to higher levels than P_{STBY}.

HIGH VOLTAGE START-UP CURRENT SOURCE

An integrated high voltage current source provides a bias current from the DRAIN pin during the start-up phase. This current is partially absorbed by internal control circuits which are

placed into a standby mode with reduced consumption and also provided to the external capacitor connected to the V_{DD} pin. As soon as the voltage on this pin reaches the high voltage threshold V_{DDon} of the UVLO logic, the device turns into active mode and starts switching. The start up current generator is switched off, and the converter should normally provide the needed current on the V_{DD} pin through the auxiliary winding of the transformer, as shown on figure 15.

In case of abnormal condition where the auxiliary winding is unable to provide the low voltage supply current to the V_{DD} pin (i.e. short circuit on the output of the converter), the external capacitor discharges itself down to the low threshold voltage V_{DDoff} of the UVLO logic, and the device get back to the inactive state where the internal circuits are in standby mode and the start up current source is activated. The converter enters a endless start up cycle, with a start-up duty cycle defined by the ratio of charging current towards discharging when the VIPer50B/BSP tries to start. This ratio is fixed by design to 2 to 15, which gives a 12% start up duty cycle while the power dissipation at start up is approximately 0.6 W, for a 230 Vrms input voltage. This low value of start-up duty cycle prevents the stress of the output rectifiers and of the transformer when in short circuit.

The external capacitor C_{VDD} on the V_{DD} pin must be sized according to the time needed by the converter to start up, when the device starts switching. This time t_{SS} depends on many parameters, among which transformer design, output capacitors, soft start feature and compensation network implemented on the COMP pin. The following formula can be used for defining the minimum capacitor needed:

$$C_{VDD} > \frac{I_{DD}\, t_{SS}}{V_{DDhyst}}$$

where:

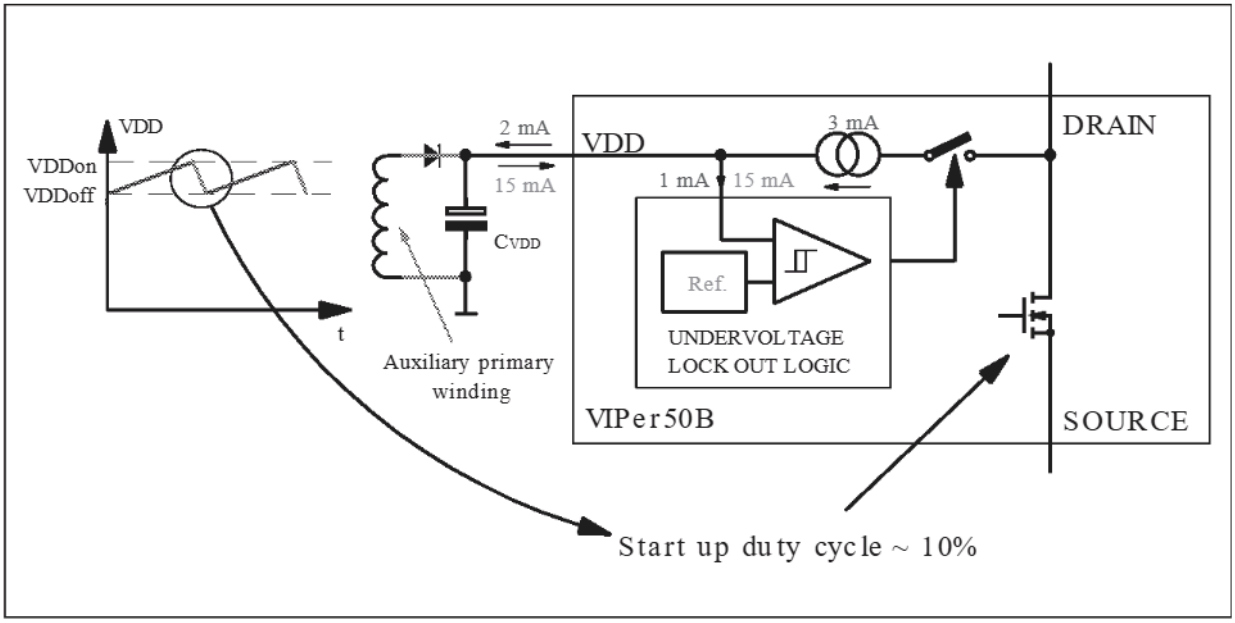
I_{DD} is the consumption current on the V_{DD} pin when switching. Refer to specified I_{DD1} and I_{DD2} values.

t_{SS} is the start up time of the converter when the device begins to switch. Worst case is generally at full load.

V_{DDhyst} is the voltage hysteresis of the UVLO logic. Refer to the minimum specified value.

Soft start feature can be implemented on the COMP pin through a simple capacitor which will be also used as the compensation network. In this case, the regulation loop bandwidth is rather low, because of the large value of this capacitor. In case a large regulation loop bandwidth is mandatory, the schematics of figure 16 can be

Figure 15: Behaviour of the high voltage current source at start-up



used. It mixes a high performance compensation network together with a separate high value soft start capacitor. Both soft start time and regulation loop bandwidth can be adjusted separately.

If the device is intentionally shut down by putting the COMP pin to ground, the device is also performing start-up cycles, and the V_{DD} voltage is oscillating between V_{DDon} and V_{DDoff}. This voltage can be used for supplying external functions, provided that their consumption doesn't exceed 0.5mA. Figure 17 shows a typical application of this function, with a latched shut down. Once the "Shutdown" signal has been activated, the device remains in the off state until the input voltage is removed.

TRANSCONDUCTANCE ERROR AMPLIFIER

The VIPer50B/BSP includes a transconductance error amplifier. Transconductance Gm is the change in output current (I_{COMP}) versus change in input voltage (V_{DD}). Thus:

$$G_m = \frac{\partial I_{COMP}}{\partial V_{DD}}$$

The output impedance Z_{COMP} at the output of this amplifier (COMP pin) can be defined as:

$$Z_{COMP} = \frac{\partial V_{COMP}}{\partial I_{COMP}} = \frac{1}{G_m} \times \frac{\partial V_{COMP}}{\partial V_{DD}}$$

This last equation shows that the open loop gain A_{VOL} can be related to G_m and Z_{COMP}:

$A_{VOL} = G_m \times Z_{COMP}$

where G_m value for VIPer50B/BSP is 1.5 mA/V typically.

G_m is well defined by specification, but Z_{COMP} and therefore A_{VOL} are subject to large tolerances. An impedance Z can be connected between the COMP pin and ground in order to define more accurately the transfer function F of the error amplifier, according to the following equation, very similar to the one above:

$F_{(S)} = Gm \times Z(S)$

The error amplifier frequency response is reported in figure 10 for different values of a simple resistance connected on the COMP pin. The unloaded transconductance error amplifier shows an internal Z_{COMP} of about 330 KΩ. More complex impedance can be connected on the COMP pin to achieve different compensation laws. A capacitor will provide an integrator function, thus eliminating the DC static error, and a resistance in series leads to a flat gain at higher frequency, insuring a correct phase margin. This configuration is illustrated on figure 18.

As shown in figure 18 an additional noise filtering capacitor of 2.2 nF is generally needed to avoid any high frequency interference.

It can be also interesting to implement a slope compensation when working in continuous mode with duty cycle higher than 50%. Figure 19 shows such a configuration. Note that R1 and C2 build the classical compensation network, and Q1 is injecting the slope compensation with the correct polarity from the oscillator sawtooth.

EXTERNAL CLOCK SYNCHRONIZATION:

The OSC pin provides a synchronisation capability, when connected to an external

Figure 16: Mixed Soft Start and Compensation

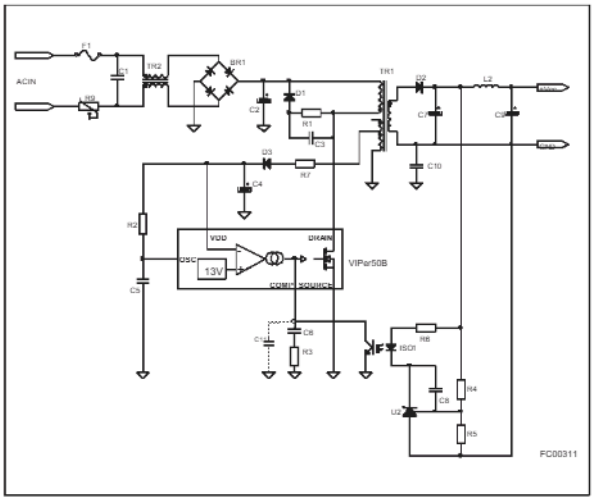
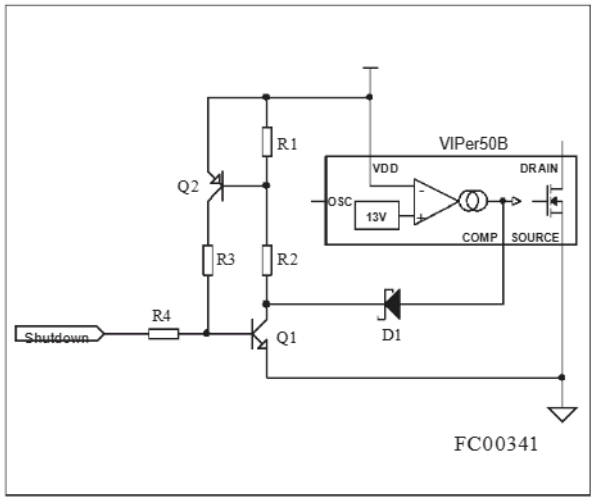


Figure 17: Latched Shut Down



frequency source. Figure 20 shows one possible schematic to be adapted depending the specific needs. If the proposed schematic is used, the pulse duration must be kept at a low value (500ns is sufficient) for minimizing consumption. The optocoupler must be able to provide 20mA through the optotransistor.

PRIMARY PEAK CURRENT LIMITATION

The primary I_{DPEAK} current and, as resulting effect, the output power can be limited using the simple circuit shown in figure 21. The circuit based on Q1, R_1 and R_2 clamps the voltage on the COMP pin in order to limit the primary peak current of the device to a value:

$$I_{DPEAK} = \frac{V_{COMP} - 0.5}{H_{ID}}$$

where:

$$V_{COMP} = 0.6 \times \frac{R_1 + R_2}{R_2}$$

The suggested value for R_1+R_2 is in the range of 220KΩ.

OVER-TEMPERATURE PROTECTION:

Over-temperature protection is based on chip temperature sensing. The minimum junction temperature at which over-temperature cut-out occurs is 140°C while the typical value is 160°C. The device is automatically restarted when the junction temperature decreases to the restart temperature threshold that is typically 40°C below

Figure 18: Typical Compensation Network

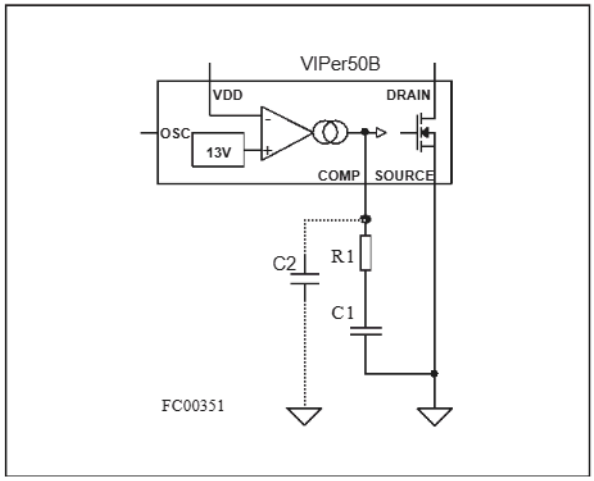


Figure 19: Slope Compensation

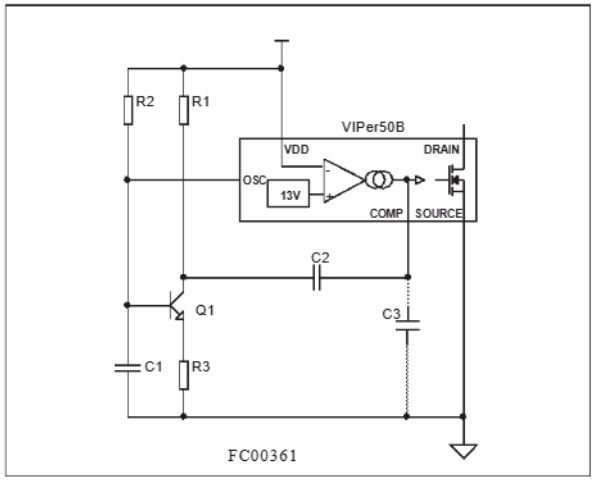


Figure 20:External Clock Synchronization

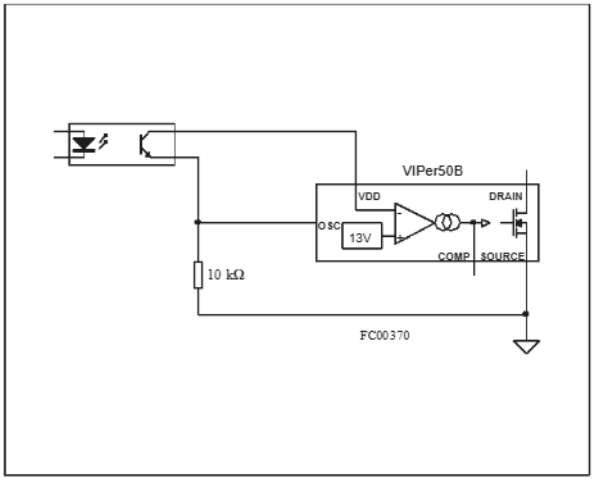


Figure 21:Current Limitation Circuit Example

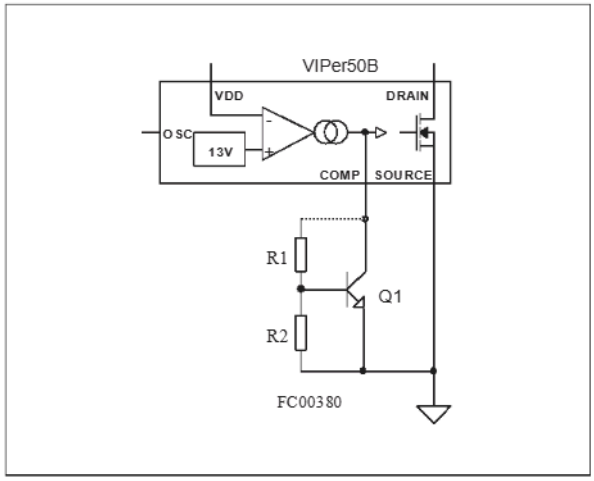
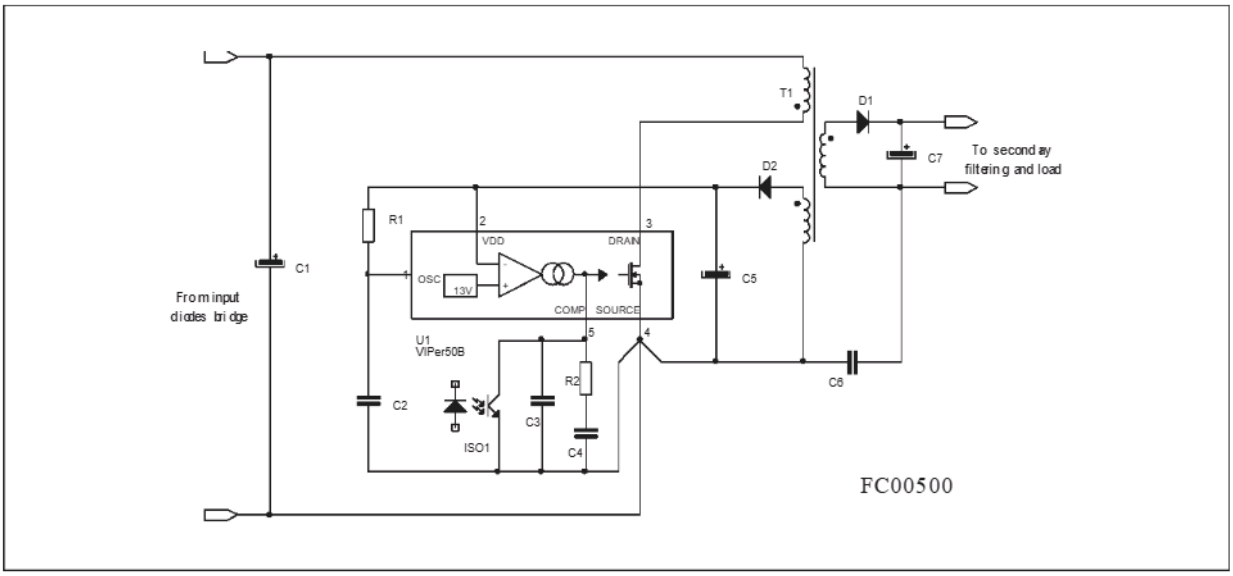


Figure 22: Recommended layout



LAYOUT CONSIDERATIONS

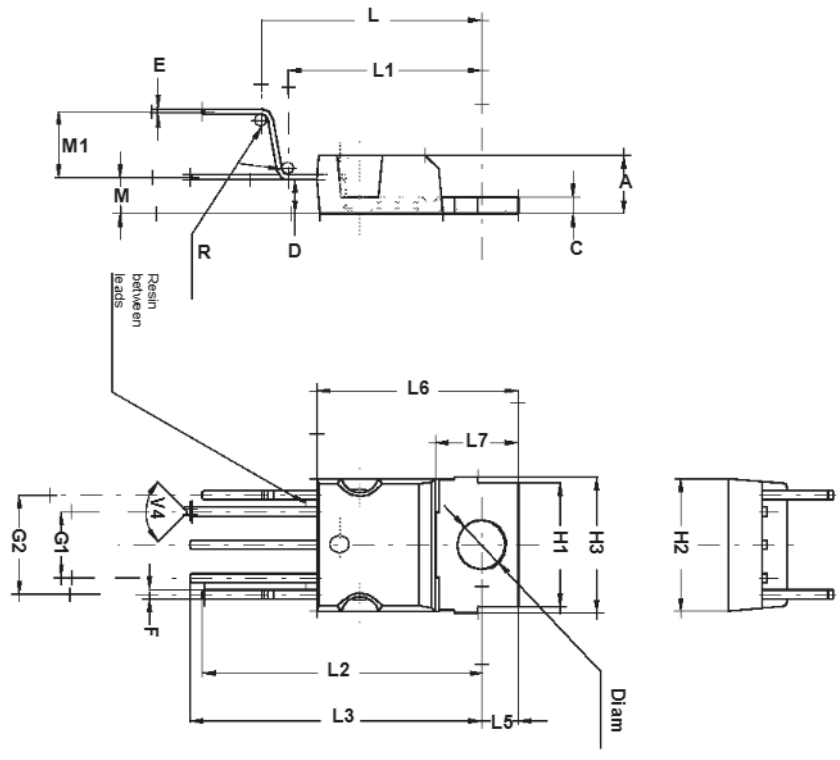
Some simple rules insure a correct running of switching power supplies. They may be classified into two categories:

- To minimise power loops: the way the switched power current must be carefully analysed and the corresponding paths must present the smallest inner loop area as possible. This avoids radiated EMC noises, conducted EMC noises by magnetic coupling, and provides a better efficiency by eliminating parasitic inductances, especially on secondary side.
- To use different tracks for low level signals and power ones. The interferences due to a mixing of signal and power may result in instabilities and/or anomalous behaviour of the device in case of violent power surge (Input overvoltages, output short circuits...).

In case of VIPer, these rules apply as shown on figure 22. The loops C1-T1-U1, C5-D2-T1, C7-D1-T1 must be minimised. C6 must be as close as possible from T1. The signal components C2, ISO1, C3 and C4 are using a dedicated track to be connected directly to the source of the device.

PENTAWATT HV (VERTICAL) MECHANICAL DATA

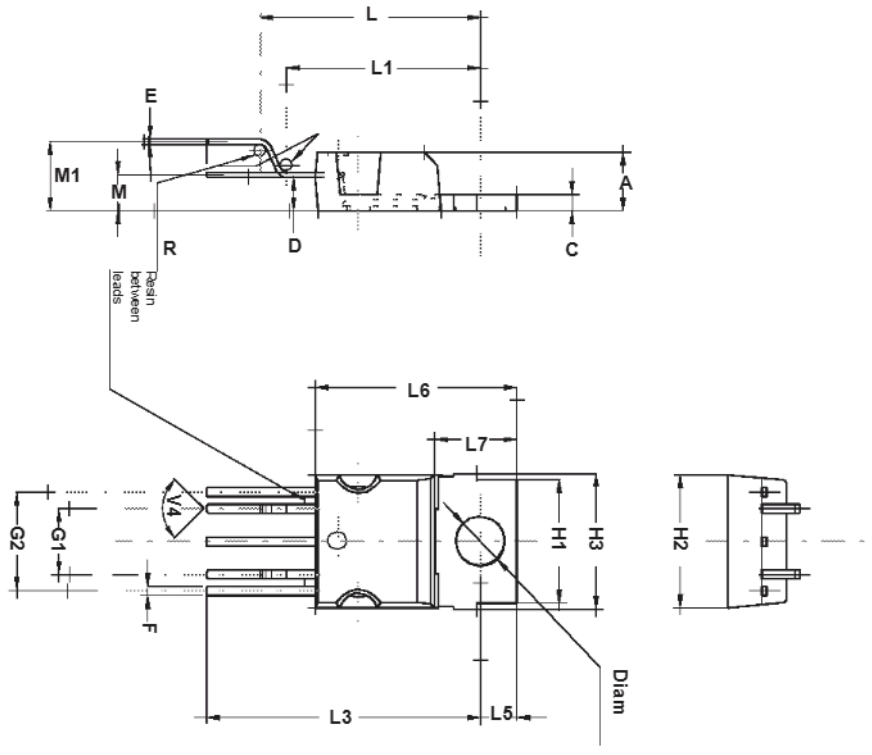
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.30		4.80	0.169		0.189
C	1.17		1.37	0.046		0.054
D	2.40		2.80	0.094		0.110
E	0.35		0.55	0.014		0.022
F	0.60		0.80	0.024		0.031
G1	4.90		5.28	0.193		0.208
G2	7.42		7.82	0.292		0.308
H1	9.30		9.70	0.366		0.382
H2			10.40			0.409
H3	10.05		10.40	0.396		0.409
L	16.60		17.30	0.653		0.681
L1	14.60		15.22	0.575		0.599
L2	21.20		21.85	0.835		0.860
L3	22.20		22.82	0.874		0.898
L5	2.60		3.00	0.102		0.118
L6	15.10		15.80	0.594		0.622
L7	6.00		6.60	0.236		0.260
M	2.50		3.10	0.098		0.122
M1	7.56		8.16	0.298		0.321
R		0.50			0.020	
V4		90°			90	
Diam.	3.70		3.90	0.146		0.154



P023H3

PENTAWATT HV 022Y(VERTICAL HIGH PITCH) MECHANICAL DATA

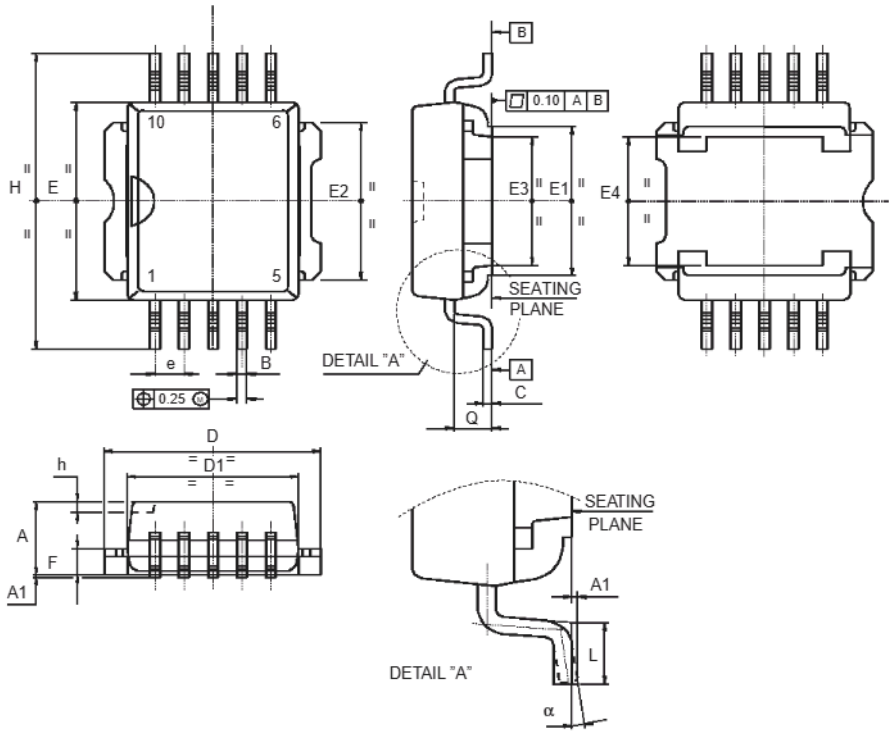
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.30		4.80	0.169		0.189
C	1.17		1.37	0.046		0.054
D	2.40		2.80	0.094		0.110
E	0.35		0.55	0.014		0.022
F	0.60		0.80	0.024		0.031
G1	4.90		5.28	0.193		0.208
G2	7.42		7.82	0.292		0.308
H1	9.30		9.70	0.366		0.382
H2			10.40			0.409
H3	10.05		10.40	0.396		0.409
L	16.42		17.42	0.646		0.686
L1	14.60		15.22	0.575		0.599
L3	20.52		21.52	0.808		0.847
L5	2.60		3.00	0.102		0.118
L6	15.10		15.80	0.594		0.622
L7	6.00		6.60	0.236		0.260
M	2.50		3.10	0.098		0.122
M1	5.00		5.70	0.197		0.224
R		0.50			0.020	
V4		90°			90°	
Diam.	3.70		3.90	0.146		0.154



P023H2

PowerSO-10 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	3.35		3.65	0.132		0.144
A1	0.00		0.10	0.000		0.004
B	0.40		0.60	0.016		0.024
C	0.35		0.55	0.013		0.022
D	9.40		9.60	0.370		0.378
D1	7.40		7.60	0.291		0.300
e		1.27			0.050	
E	9.30		9.50	0.366		0.374
E1	7.20		7.40	0.283		0.291
E2	7.20		7.60	0.283		0.300
E3	6.10		6.35	0.240		0.250
E4	5.90		6.10	0.232		0.240
F	1.25		1.35	0.049		0.053
h		0.50			0.002	
H	13.80		14.40	0.543		0.567
L	1.20		1.80	0.047		0.071
q		1.70			0.067	
α	0°		8°			



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