TLE8104E

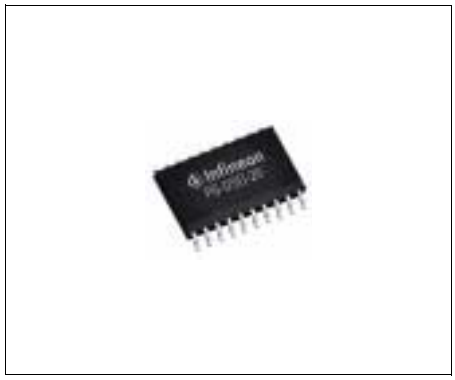
Smart Quad Channel Powertrain Switch coreFLEX

Automotive Power

Never stop thinking

Table of Contents

1 Overview



PG-DSO-20-30

Features

- Overload Protection
- DMOS Overtemperature protection
- Overvoltage protection
- Open load detection
- Low quiescent current mode
- **E**lectro**s**tatic **d**ischarge (ESD) protection
- IC Overtemperature warning
- 8-Bit SPI (for diagnosis and control)
- Short to GND detection
- Green Product (RoHS compliant)
- AEC Qualified

Description

Quad Low-Side Switch in Smart Power Technology (SPT) with four open drain DMOS output stages. The TLE8104E is protected by embedded protection functions and designed for automotive applications. The output stages can be controlled directly by parallel inputs for PWM applications (e.g. gasoline port injection) or by SPI. The parallel inputs can be programmed to be active high or active low. Diagnosis can be read from an 8-bit SPI or by the external fault pin.

Type	Package	Marking
TLE8104E	PG-DSO-20-30	TLE8104E

Table 1 Product Summary

Operating voltage	V_S	4.5 … 5.5 V
Drain source voltage	$V_{DS(AZ)}$	45 … 60 V
Typical On-state resistance CH 1 - 4 at T_j = 25°C	$R_{DS(ON)}$	320 mΩ
Maximum On-state resistance CH 1 - 4 at T_j = 150°C	$R_{DS(ON)}$	650 mΩ
Nominal load current CH 1 - 4	I_D	1 A
Minimum current limitation CH 1 - 4	$I_{D\ (lim)}$	3 A

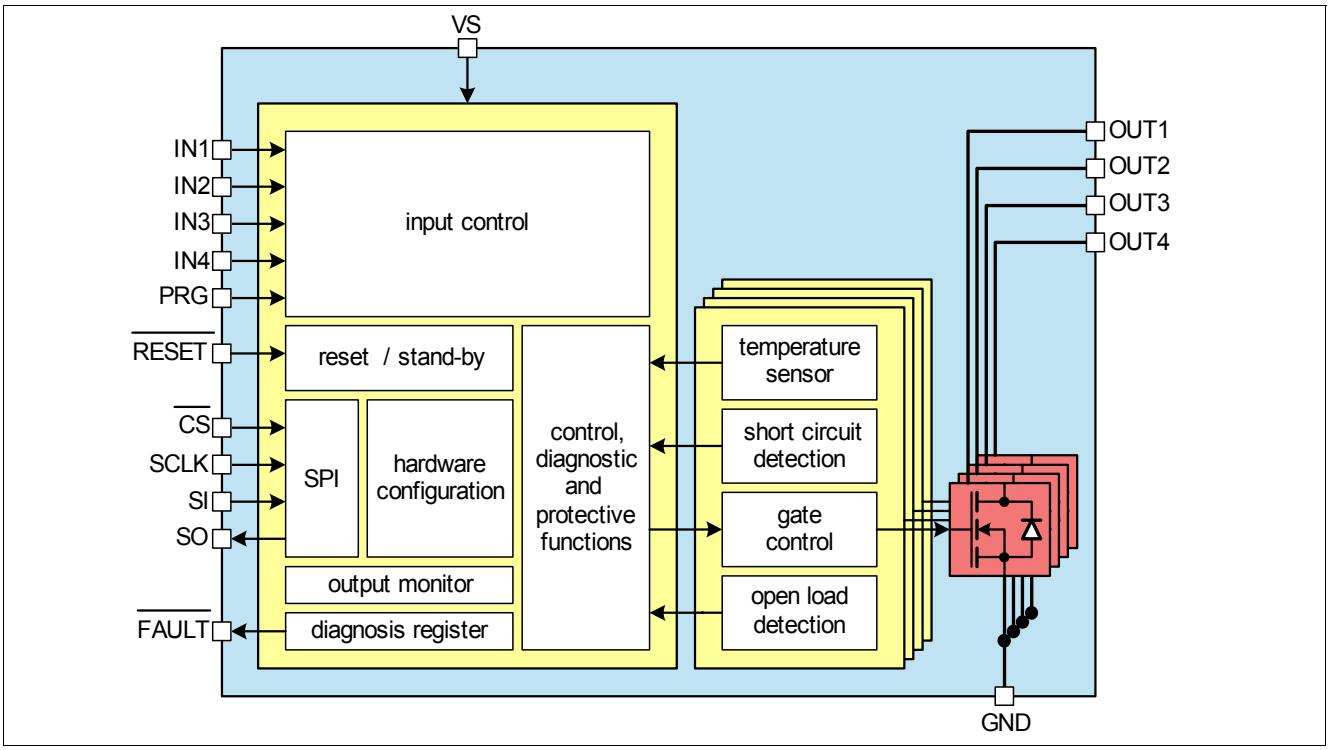


Figure 1 Block Diagram

2 Terms

Figure 2 shows all terms used in this Data Sheet.

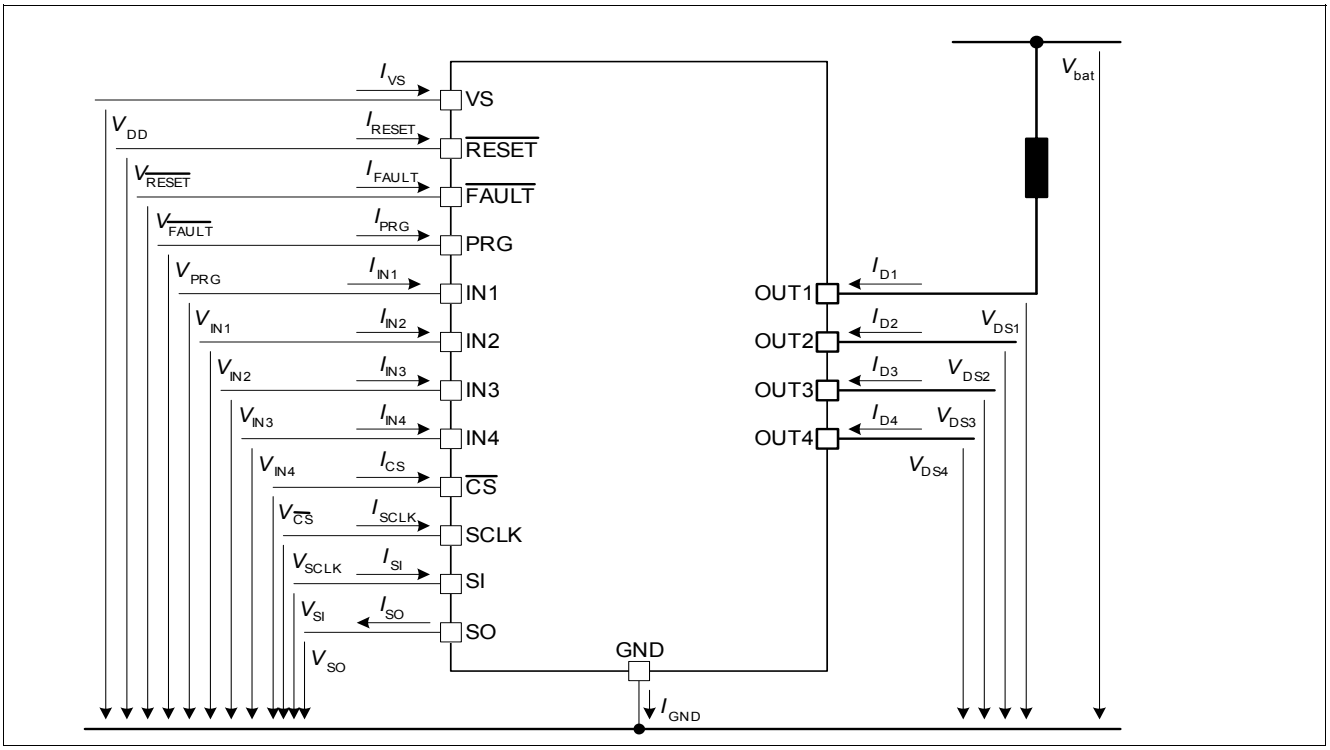


Figure 2 Terms

The following is valid for all electrical characteristics cables: Channel related symbols without channel number are valid for each channel separately (e.g. V_{DS} specification is valid for V_{DS1}, V_{DS2}, V_{DS3} and V_{DS4}).

3 Pin Configuration

3.1 Pin Assignment

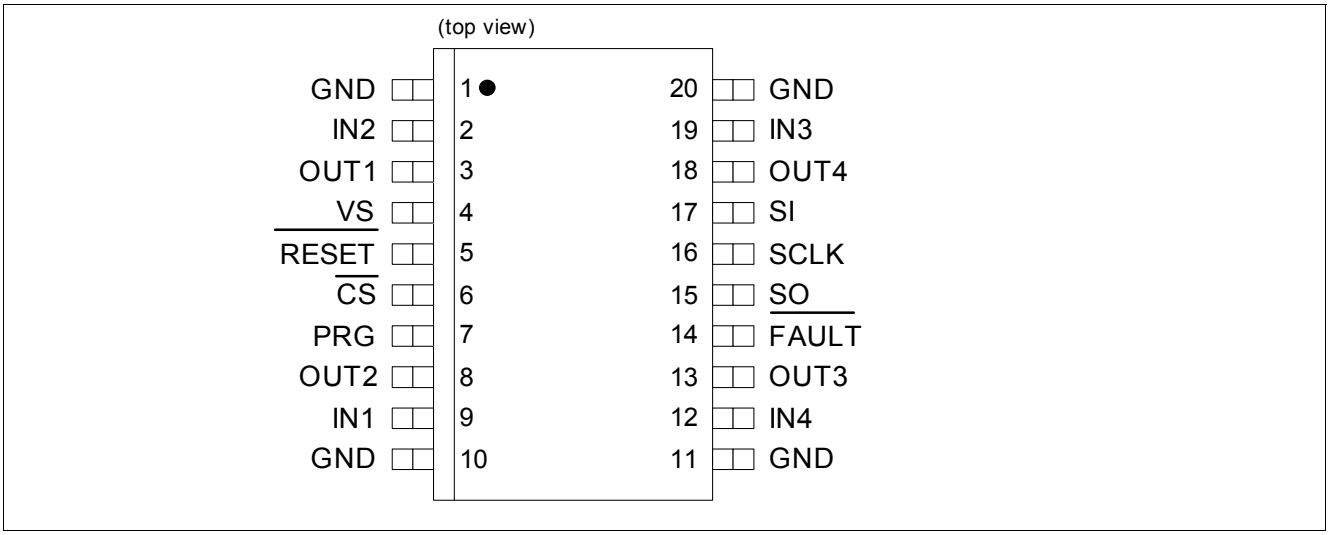


Figure 3 Pin Configuration (top view)

All GND pins and the heat sink must be connected to GND externally.

3.2 Pin Definitions and Functions

Pin	Symbol	Function
1	GND	**Ground**
2	IN2	**Input Channel 2**
3	OUT1	**Power Output Channel 1**
4	VS	**Supply Voltage**
5	$\overline{\text{RESET}}$	**Reset Input**
6	$\overline{\text{CS}}$	**SPI Chip Select**
7	PRG	**Program Input**
8	OUT2	**Power Output Channel 1**
9	IN1	**Input Channel 1**
10	GND	**Ground**
11	GND	**Ground**
12	IN4	**Input Channel 4**
13	OUT3	**Power Output Channel 3**
14	$\overline{\text{FAULT}}$	**Fault Output**
15	SO	**SPI Signal Out**
16	SCLK	**SPI Clock**
17	SI	**SPI Signal In**
18	OUT4	**Power Output Channel 4**
19	IN3	**Input Channel 3**
20	GND	**Ground**

4 Maximum Ratings and Operating Conditions

4.1 Absolute Maximum Ratings

Absolute Maximum Ratings [1)]

T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
4.1.1	Supply Voltage	V_S	-0.3	7	V	–
4.1.2	Continuous Drain Source Voltage (OUT1 to OUT4)	V_{DS}	-0.3	45	V	–
4.1.3	Input Voltage, All Inputs and Data outputs, Sense Lines	V_{IN}	-0.3	7	V	–
4.1.4	Output Current per Channel[2)]	I_D	0	3	A	Output ON
4.1.5	Maximum Voltage for short circuit Protection (single event)[3)]	$V_{SC, single}$	–	30	V	
4.1.6	**E**lectro**s**tatic **D**ischarge Voltage (human body model) according to EIA/JESD22-A114-E	V_{ESD}	-2000	2000	V	

1) Not subject to production test, specified by design.

2) Output current rating as long as maximum junction temperature is not exceeded. The maximum output current in the application has to be calculated using R_{thJA} depending on mounting conditions.

3) Device mounted on PCB (100 mm × 100 mm × 1.5 mm epoxy, FR4); PCB in test chamber without blown air. All channels have identical loads.

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

4.2 Operating Conditions

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
4.2.1	Output Clamping Energy (single event), linearly decreasing current[1]	E_{AS}	–	–	50	mJ	$I_{D(0)}$ = 1 A, $T_{J(0)}$ = 150 °C
Thermal Resistance							
4.2.2	Junction to case	R_{thJSP}	–	2.1	3	K/W	P_V = 3W
4.2.3	Junction to ambient, all channels active[2]	R_{thJA}	–	26.2	–	K/W	P_V = 3W
Temperature Range							
4.2.4	Operating Temperature Range	T_j	-40	–	150	°C	–
4.2.5	Storage Temperature Range	T_{stg}	-55	–	150	°C	–

1) Pulse shape represents inductive switch off: $I_{D(t)} = I_{D(0)} \times (1 - t / t_{pulse})$; $0 < t < t_{pulse}$

2) PCB set-up according **Figure 4**

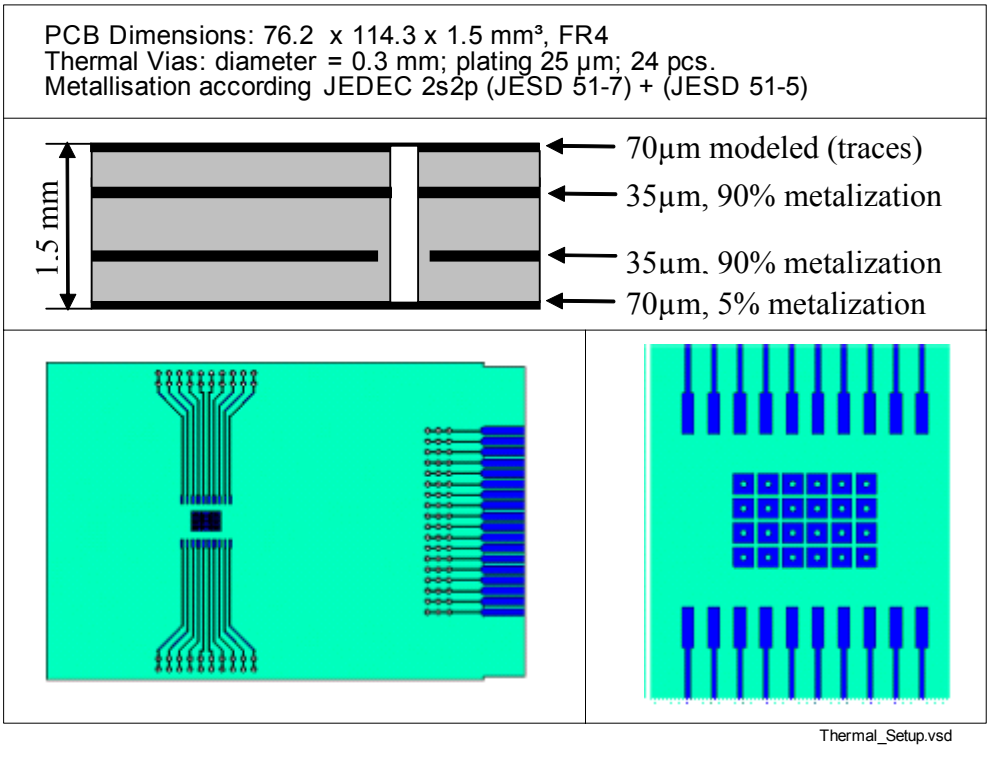


Figure 4 Thermal Simulation - PCB setup

Note: Within the functional range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given by the related electrical characteristics table.

5 Electrical and Functional Description of Blocks

5.1 Power Supply

The TLE8104E is supplied by power supply line V_S, used for the digital as well as the analog functions of the device including the gate control of the power stages. A capacitor between pins VS to GND is recommended.

A $\overline{\text{RESET}}$ pin is available. When a low level is applied to this pin, the device enters sleep mode. In this case, all registers are set to their default values and the quiescent supply current is minimized.

After start-up of the power supply, the $\overline{\text{RESET}}$ pin should be kept low until the Reset Duration Time has expired, reseting all SPI registers to their default values.

Electrical Characteristics: Power Supply

V_S = 4.5 V to 5.5 V, T_j = -40 °C to +150 °C, (unless otherwise specified)
all voltages with respect to ground, positive current flowing into pin

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.1.1	Supply Voltage	V_S	4.5	–	5.5	V	–
5.1.2	Supply Current	$I_{S(ON)}$	–	1	2	mA	all channels ON
5.1.3	Supply Current in Sleep Mode	$I_{S(sleep)}$	–	–	100	µA	V_{RESET} = 0 V V_{INn} = 0 V V_{SCLK} = 0 V V_{SI} = 0 V V_{CS} = V_S V_{PRG} = V_S V_{FAULT} = V_S
5.1.4	Input Low Voltage of pin $\overline{\text{RESET}}$	$V_{RESET(L)}$	-0.3	–	1.0	V	–
5.1.5	Input High Voltage of pin $\overline{\text{RESET}}$	$V_{RESET(H)}$	2.0	–	V_S +0.3	V	–
5.1.6	Low Input Pull-up Current through pin $\overline{\text{RESET}}$	$I_{RESET(L)}$	20	50	100	µA	V_{RESET} = 0 V,
5.1.7	Reset duration time[1)]	$t_{RESET(L)}$	10	–	–	µs	–

1) For proper startup, after the supply V_S has reached its final voltage, the $\overline{\text{RESET}}$ pin should be held low until the reset duration time has expired.

5.2 Parallel Inputs

Each input signal controls the output stages of its assigned channel. For example, IN1 controls OUT1, IN2 controls OUT2, etc. Please refer to **Figure 4** for details.

The PRG pin selects if the input pins are active high or active low and activates either a pull-down or pull-up current source. If PRG is high, the input pins are active high and the pull-down current source is active. If PRG is low, the input pins are active low and the pull-up current source is active. The respective current sources at the input pin ensure that the channels switch off in case of an unconnected pin. The zener diode protects the input circuit against ESD pulses.

The BOL bit can be set via SPI. This bit determines if a Boolean OR or AND operation is performed on the INn signals and their corresponding data bits CHn_{IN}. The default setting of the BOL bit programs the device to perform an OR operation.

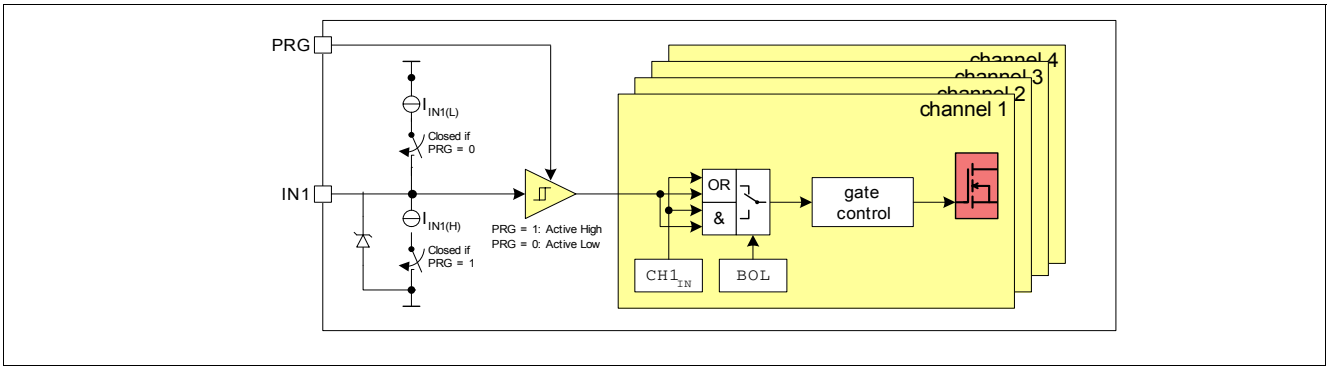


Figure 4 Input Control and Boolean Operator

Electrical Characteristics: Parallel Inputs

V_S = 4.5 V to 5.5 V, T_j = -40 °C to +150 °C, (unless otherwise specified)
all voltages with respect to ground, positive current flowing into pin

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.2.1	Input Low Voltage of pin INn	V_{INL}	-0.3	–	1.0	V	–
5.2.2	Input High Voltage of pin INn	V_{INH}	2.0	–	V_S +0.3	V	–
5.2.3	Input Voltage Hysteresis[1)]	V_{INHys}	50	100	200	mV	–
5.2.4	Low Input Pull-up Current through pin INn	$I_{IN(L)}$	20	50	100	µA	V_{IN} = 0 V, PRG = 0
5.2.5	High Input Pull-down Current through pin INn	$I_{IN(L)}$	20	50	100	µA	V_{IN} = V_S, PRG = 1
5.2.6	Input Low Voltage of pin PRG	$V_{PRG(L)}$	-0.3	–	1.0	V	–
5.2.7	Input High Voltage of pin PRG	$V_{PRG(H)}$	2.0	–	V_S +0.3	V	–
5.2.8	Low Input Pull-up Current through pin PRG	$I_{PRG(L)}$	20	50	100	µA	V_{PRG} = 0 V,

1) Not subject to production test, specified by design.

5.3 Power Outputs

5.3.1 Electrical Characteristics

Electrical Characteristics: Power Outputs

V_S = 4.5 V to 5.5 V, T_j = -40 °C to +150 °C, (unless otherwise specified)
all voltages with respect to ground, positive current flowing into pin

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.3.1	ON Resistance	$R_{DS(ON)}$	–	0.32	–	Ω	T_J = 25 °C, V_S = 5 V, I_D = 1A
			–	0.52	0.65	Ω	T_J = 150 °C, V_S = 5 V, I_D = 1A
5.3.2	Output Clamping Voltage	$V_{DS(AZ)}$	45	53	60	V	output OFF
5.3.3	Over load current limitation	$I_{D(lim)}$	3	4.5	6	A	V_{DS} = 12 V
5.3.4	Output Leakage Current	$I_{D(lkg)}$	–	–	10	µA	T_J = 150 °C, V_{DS} = 35 V, V_S = 5 V, $\overline{\text{RESET}}$ = 0
5.3.5	Turn-On Time	t_{ON}	– –	5	10	µs	I_D = 1 A, resistive load
5.3.6	Turn-Off Time	t_{OFF}	– –	5	10	µs	I_D = 1 A, resistive load
5.3.7	Over temperature shutdown threshold[1)]	$T_{j(OT)}$	170	–	200	°C	–
5.3.8	Over temperature restart hysteresis[1)]	$\Delta T_{j(OT)}$	–	10	–	K	–

1) Not subject to production test, specified by design.

5.3.2 Timing Diagrams

The power transistors are switched on and off with a dedicated slope either via the parallel inputs or by the CHn_{IN} bits of the serial peripheral interface SPI. The switching times t_{ON} and t_{OFF} are designed equally. See **Figure 5** for details

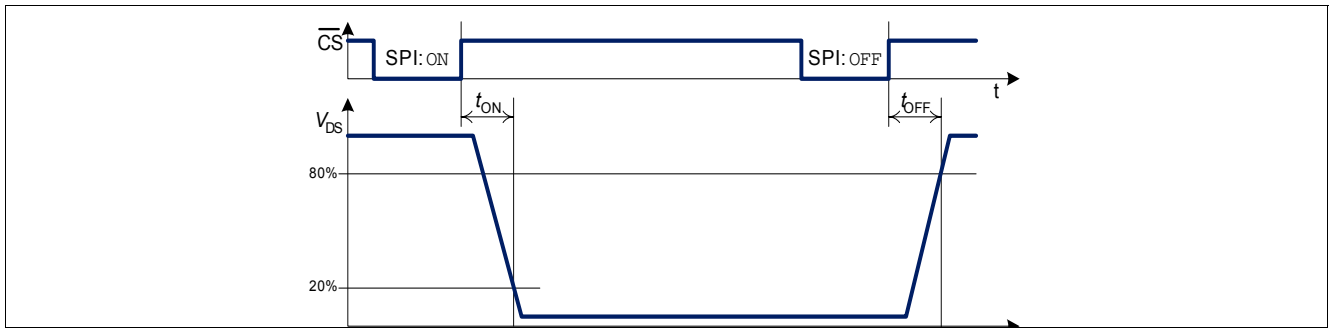


Figure 5 Switching a Resistive Load

5.3.3 Inductive Output Clamp

When switching off inductive loads, the potential at pin OUT rises to $V_{DS(CL)}$, as the inductance continues to drive current. The inductive output clamp is necessary to prevent destruction of the device. See **Figure 6** for details. The maximum allowed load inductance and current, however, are limited.

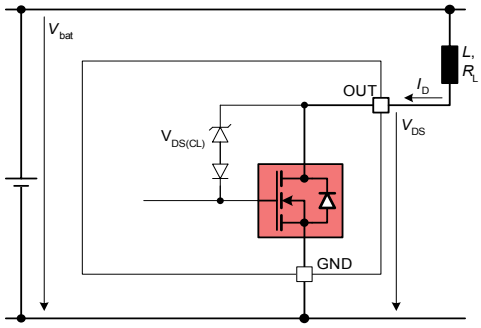


Figure 6 Inductive Output Clamp

Maximum Load Inductance

During demagnetization of inductive loads, energy has to be dissipated in the TLE8104E. This energy can be calculated with following equation:

$$E = V_{DS(CL)} \cdot \left[\frac{V_{bat} - V_{DS(CL)}}{R_L} \cdot \ln\left(1 - \frac{R_L \cdot I_D}{V_{bat} - V_{DS(CL)}}\right) + I_D \right] \cdot \frac{L}{R_L}$$

The equation simplifies under the assumption of R_L = 0:

$$E = \frac{1}{2} L I_D^2 \cdot \left(1 - \frac{V_{bat}}{V_{bat} - V_{DS(CL)}}\right)$$

The energy, which is converted into heat, is limited by the thermal design of the component.

5.3.4 Protection Functions

The TLE8104E provides embedded protective functions. Integrated protection functions are designed to prevent IC destruction under fault conditions described in this data sheet. Fault conditions are considered “outside” the normal operating range. Protection functions are not designed for continuous repetitive operation.

Over load and over temperature protections are implemented in the TLE8104E. **Figure 7** gives an overview of the protective functions.

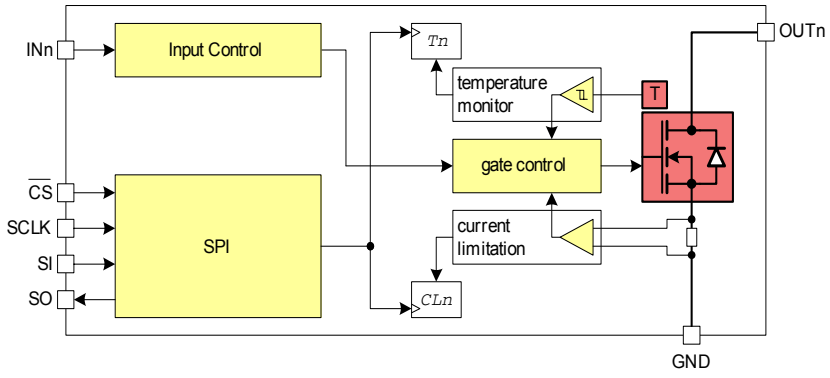


Figure 7 Protection Functions

5.3.4.1 Over Load Protection

The TLE8104E is protected in case of over load or short circuit of the load. The current is limited to $I_{DS(lim)}$. After time $t_{d(\overline{fault})}$, the corresponding over load flag CLn is set. The channel may shut down due to over temperature.

The over load flag (CLn) of the affected channel is cleared by the rising edge of the $\overline{CS}$ signal after a successful SPI transmission. For timing information, please refer to **Figure 8** for details.

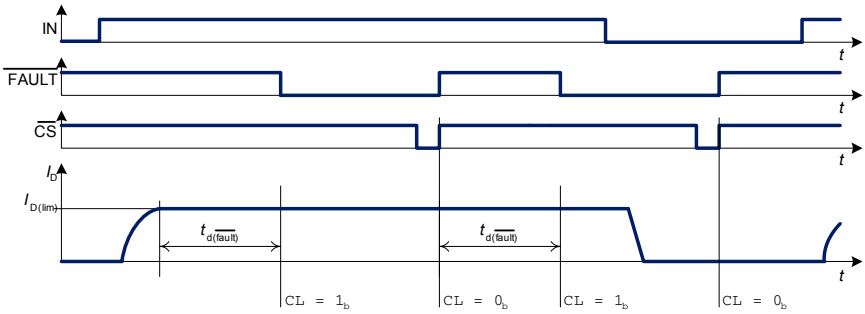


Figure 8 Over Load Behavior

5.3.4.2 Over Temperature Protection

A dedicated temperature sensor for each channel detects if the temperature of its channel exceeds the over temperature shutdown threshold. If the channel temperature exceeds the over temperature shutdown threshold, the overheated channel is switched off immediately to prevent destruction. At the same time (no delay), the over temperature flag Tn is set. After cooling down, the channel is switched on again with thermal hysteresis ΔT_j.

The over temperature flag of the affected channel is cleared by the rising edge of the $\overline{CS}$ signal after a successful SPI transmission.

5.3.5 Reverse Polarity Protection

In the case of reverse polarity when outputs are turned off, the intrinsic body diode of the power transistor causes power dissipation. The reverse current through the intrinsic body diode has to be limited by the connected load. The V_S supply pin must be protected against reverse polarity externally. Please note that neither the over load nor over temperature are functional in reverse current operation.

5.4 Diagnostic Functions

The TLE8104E provides diagnosis information about the device and about the load. The following diagnosis functions are implemented:

- The protective functions (flags *CLn* and *Tn*) of channel n are registered in the diagnosis flag *Pn*.
- The open load diagnosis of channel n is registered in the diagnosis flag *OLn*.
- The short to ground monitor information of channel n is registered in the diagnosis flag *SGn*

The diagnosis information of the TLE8104E can either be accessed by the SPI interface or $\overline{\text{FAULT}}$ pin. With the exception of over temperature, a fault is only recognized if it lasts longer than the fault delay time $t_{d(\overline{fault})}$. When using the SPI interface and fault pin, diagnosis flags are latched in the diagnosis register of the SPI interface. In this case, diagnosis flags are cleared by the rising edge of the $\overline{\text{CS}}$ signal after a successful SPI transmission.

Please see **Figure 9** for details.

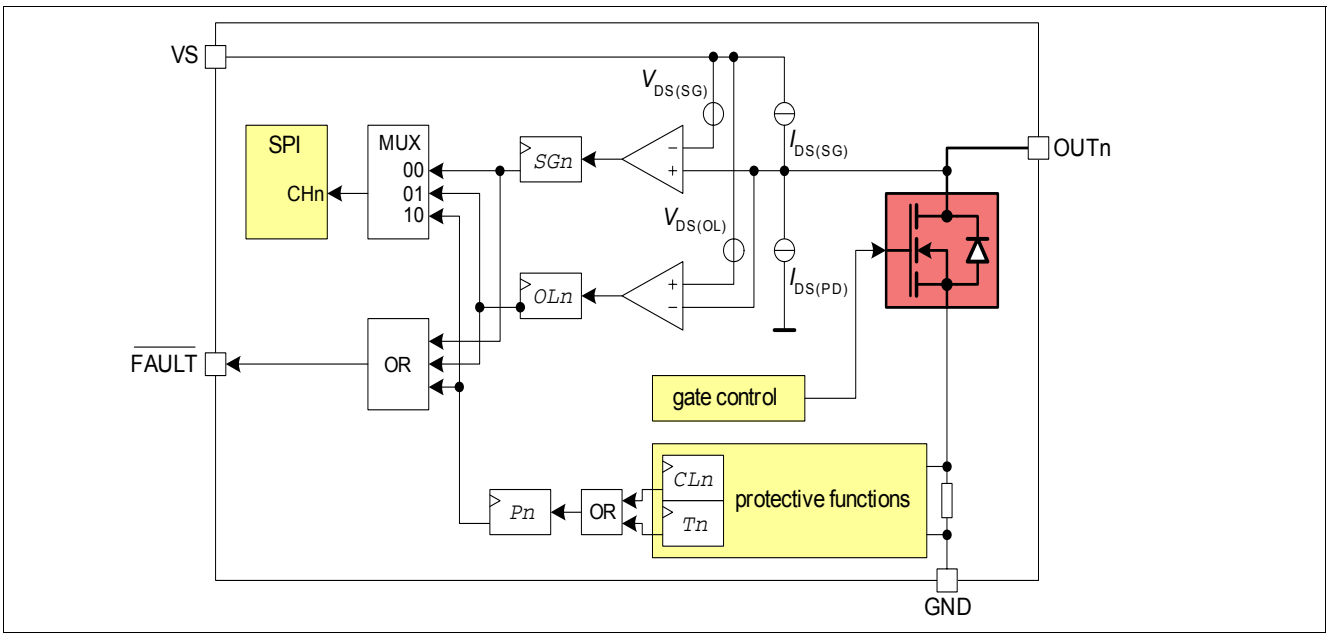


Figure 9 Block Diagram of Diagnostic Functions

Electrical Characteristics: Diagnostic Functions

V_S = 4.5 V to 5.5 V, T_j = -40 °C to +150 °C, (unless otherwise specified)
all voltages with respect to ground, positive current flowing into pin

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.4.1	Open Load Detection Voltage (Channel OFF)	$V_{DS(OL)}$	V_S - 2.5	V_S - 2.0	V_S - 1.3	V	–
5.4.2	Output Pull-down Current (Channel OFF)	$I_{PD(OL)}$	50	90	150	µA	V_{DS} = 32 V
5.4.3	Short to Ground Detection Voltage	$V_{DS(SHG)}$	V_S - 3.3	V_S - 2.9	V_S - 2.5	V	–
5.4.4	Output Pull-up Current (Channel OFF)	$I_{PU(SHG)}$	-50	-100	-150	µA	V_{DS} = 0 V
5.4.5	$\overline{\text{FAULT}}$ Filtering Time	$t_{d(\overline{fault})}$	50	110	200	µs	–
5.4.6	Low level output voltage of pin $\overline{\text{FAULT}}$	V_{FAULT}	0	–	0.4	V	I_{FAULT} = 1.6 mA

5.5 SPI Interface

The diagnosis and control interface is based on a serial peripheral interface (SPI).

The SPI is a full duplex synchronous serial slave interface, which uses four lines: SO, SI, SCLK and $\overline{CS}$. Data is transferred by the lines SI and SO at the data rate given by SCLK. The falling edge of $\overline{CS}$ indicates the beginning of a data access. Data is sampled in on line SI at the falling edge of SCLK and shifted out on line SO at the rising edge of SCLK. Each access must be terminated by a rising edge of $\overline{CS}$. A modulo 8 counter ensures that data is taken only, when a multiple of 8 bit has been transferred. The interface provides daisy chain capability.

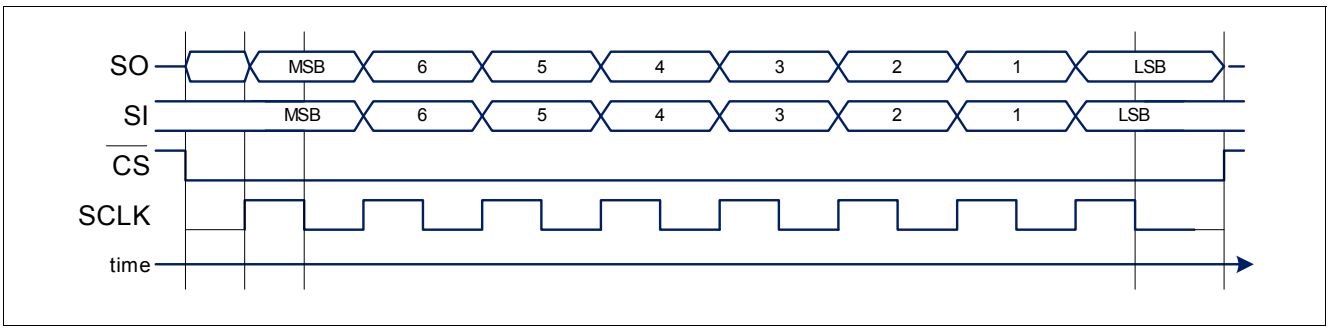


Figure 10 Serial Peripheral Interface

The SPI protocol is described in **Section 6**. All registers are reset to default values after power-on reset or if the chip is programmed via SPI to enter sleep mode.

5.5.1 SPI Signal Description

$\overline{CS}$ - Chip Select: The system micro controller selects the TLE8104E by means of the $\overline{CS}$ pin. Whenever the pin is in low state, data transfer can take place. When $\overline{CS}$ is in high state, any signals at the SCLK and SI pins are ignored and SO is forced into a high impedance state.

$\overline{CS}$ High to Low transition: ⎺_

- The diagnosis information is transferred into the shift register.

$\overline{CS}$ Low to High transition: _/⎺

- Command decoding is only done after the falling edge of $\overline{CS}$ and a exact multiple (1, 2, 3, …) of eight SCLK signals have been detected.
- Data from shift register is transferred into the input matrix register.
- The diagnosis flags are cleared.

SCLK - Serial Clock: This input pin clocks the internal shift register. The serial input (SI) transfers data into the shift register on the falling edge of SCLK while the serial output (SO) shifts diagnostic information out on the rising edge of the serial clock. It is essential that the SCLK pin is in low state whenever chip select $\overline{CS}$ makes any transition.

SI - Serial Input: Serial input data bits are shifted in at this pin, the most significant bit first. SI information is read on the falling edge of SCLK. The 8 bit input data consist of two parts (control and data). Please refer to **Section 6** for further information.

SO - Serial Output: Data is shifted out serially at this pin, the most significant bit first. SO is in high impedance state until the $\overline{CS}$ pin goes to low state. New data will appear at the SO pin following the rising edge of SCLK. Please refer to **Section 6** for further information.

5.5.2 Daisy Chain Capability

The SPI of TLE8104E is daisy chain capable. In this configuration several devices are activated by the same signal $\overline{CS}$. The SI line of one device is connected with the SO line of another device (see **Figure 11**), which builds a chain. The ends of the chain are connected with the output and input of the master device, SO and SI respectively. The master device provides the master clock SCLK, which is connected to the SCLK line of each device in the chain.

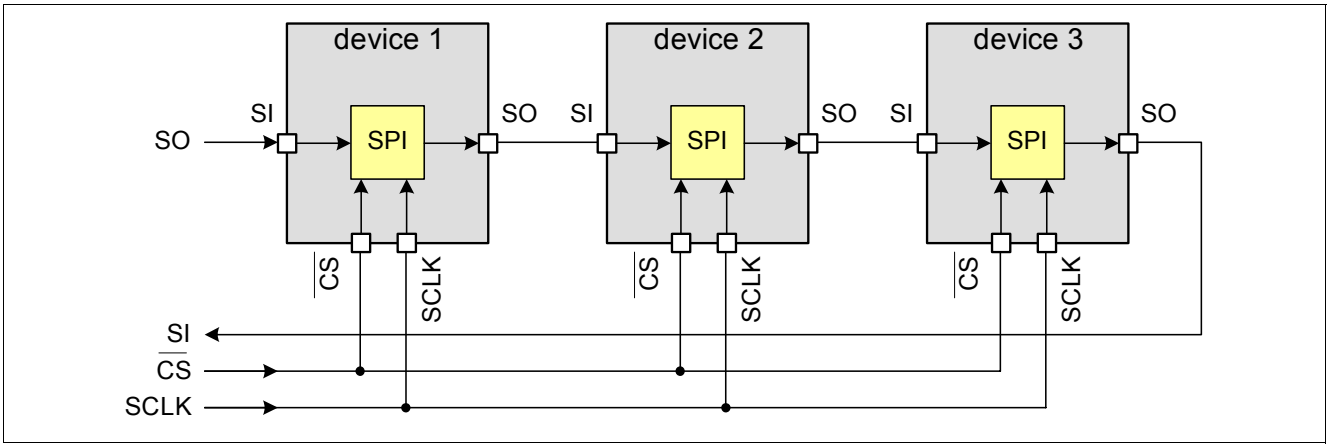


Figure 11 Daisy Chain Configuration

In the SPI block of each device, there is one shift register where one bit from SI line is shifted in each SCLK. The bit shifted out can be seen at SO. After 8 SCLK cycles, the data transfer for one device has been finished. In single chip configuration, the $\overline{CS}$ line must go high to make the device accept the transferred data. In daisy chain configuration the data shifted out at device 1 has been shifted in to device 2. When using three TLE8104E devices in daisy chain, three times 8 bits have to be shifted through the devices. After that, the $\overline{CS}$ line must go high (see **Figure 12**).

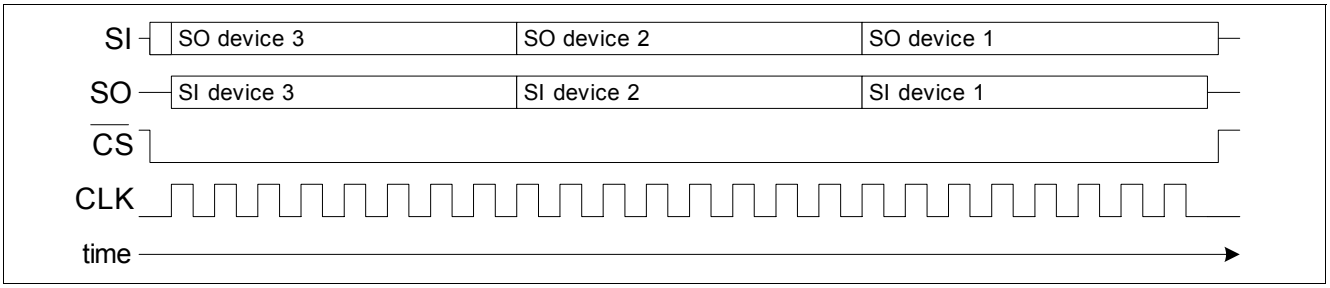


Figure 12 Data Transfer in Daisy Chain Configuration

Electrical Characteristics: SPI Interface

V_S = 4.5 V to 5.5 V, T_j = -40 °C to +150 °C, (unless otherwise specified)
all voltages with respect to ground, positive current flowing into pin

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.5.1	Input Pull-down Current (SI, SCLK)	$I_{IN(SI,SCLK)}$	10	20	50	µA	$V_{SI,SCLK} = V_S$
5.5.2	Input Pull-up Current ($\overline{CS}$)	$I_{IN(\overline{CS})}$	10	20	50	µA	V_{CS} = 0 V
5.5.3	SO High State Output Voltage	V_{SOH}	V_S - 0.4	–	–	V	I_{SOH} = 2 mA
5.5.4	SO Low State Output Voltage	V_{SOL}	–	–	0.4	V	I_{SOL} = 2.5 mA
5.5.5	Serial Clock Frequency (depending on SO load)	f_{SCK}	DC	–	5	MHz	–

Electrical Characteristics: SPI Interface (cont'd)

V_S = 4.5 V to 5.5 V, T_j = -40 °C to +150 °C, (unless otherwise specified)
all voltages with respect to ground, positive current flowing into pin

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.5.6	Serial Clock Period ($1/f_{sclk}$)	$t_{p(SCK)}$	200	–	–	ns	–
5.5.7	Serial Clock High Time	t_{SCKH}	50	–	–	ns	–
5.5.8	Serial Clock Low Time	t_{SCKL}	50	–	–	ns	–
5.5.9	Enable Lead Time (falling edge of $\overline{CS}$ to rising edge of SCLK)	t_{lead}	250	–	–	ns	–
5.5.10	Enable Lag Time (falling edge of SCLK to rising edge of $\overline{CS}$)	t_{lag}	250	–	–	ns	–
5.5.11	Data Setup Time (required time SI to falling of SCLK)	t_{SU}	20	–	–	ns	–
5.5.12	Data Hold Time (falling edge of SCLK to SI)	t_H	20	–	–	ns	–
5.5.13	Disable Time[1)]	t_{DIS}	–	–	150	ns	–
5.5.14	Transfer Delay Time[2)] ($\overline{CS}$ high time between two accesses)	t_{dt}	200	–	–	ns	–
5.5.15	Data Valid Time[3)]	t_{valid}	–	–	110	ns	C_L = 50 pF

1) Not subject to production test, specified by design.

2) This time is necessary between two write accesses. To get the correct diagnostic information, the transfer delay time has to be extended to the maximum fault delay time $t_{d(\overline{fault})max}$ = 200 µs.

3) Not subject to production test, specified by design.

5.6 Timing Diagrams

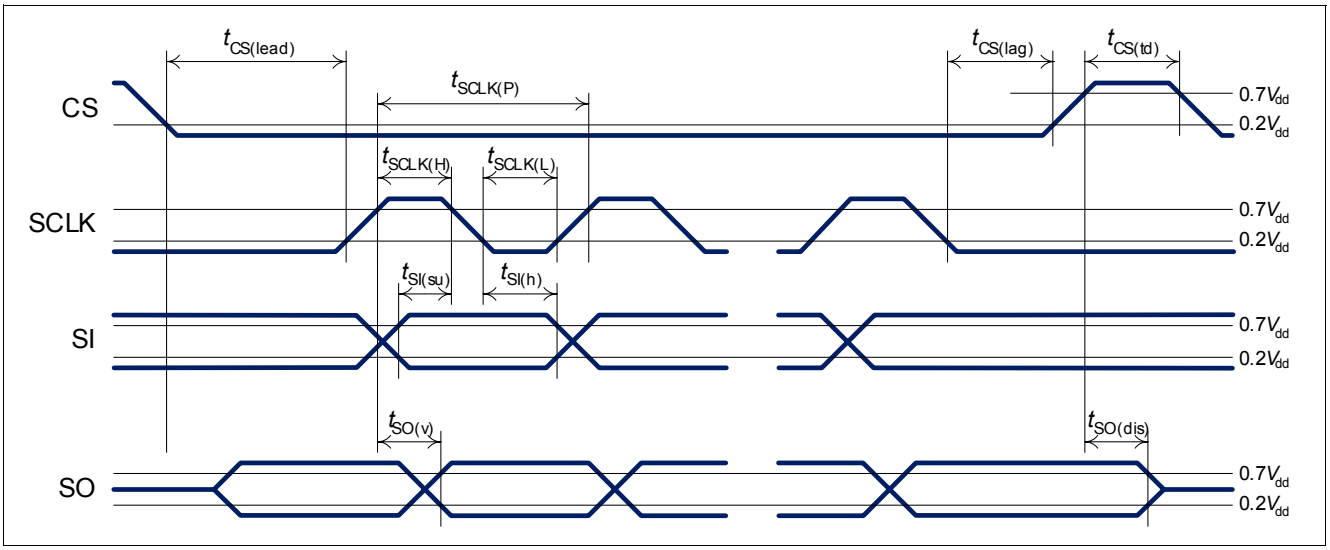


Figure 13 Serial Interface Timing Diagram

6 SPI Control

The SPI protocol of the TLE8104E provides two types of registers: control and diagnosis. After power-on reset, all register bits are set to default values.

Serial Input
Default Value: 00_H

7	6	5	4	3	2	1	0
CMD				**DATA** ($CH4_{IN}$ $CH3_{IN}$ $CH2_{IN}$ $CH1_{IN}$)			
w	w	w	w	w	w	w	w

Field	Bits	Type	Description
CMD	7:4	w	**Command** 0000 Diagnosis only 1100 Read back input and 1-bit diagnosis 1010 Echo function of SPI 0011 *BOL* bit set for logic OR operation of *INn* and data bits. The default value for the *BOL* bit is logic OR. 1111 *BOL* bit set for logic AND operation of *INn* and data bits XXXX All other command words are accepted as an OR or AND command with valid data bits depending on the previously programmed Boolean operation.
DATA	3:0	w	**Data** If Command is 0000 Data bits are ignored. If Command is 1100 Data bits are ignored. If Command is 1010 Data bits will appear as bits 3:0 at SO during the next CS period. If Command is 0011 Each of the data bits is OR'ed with its corresponding input signal *INn*. If Command is 1111 Each of the data bits is AND'ed with its corresponding input signal *INn*. All other Commands Each of the data bits is OR'ed or AND'ed with its corresponding input signal *INn*, depending on the previously programmed Boolean operation.

Serial Output (Standard Diagnosis)
Default Value: FF_H

7	6	5	4	3	2	1	0
CH4 ($CH4_1$ $CH4_0$)		**CH3** ($CH3_1$ $CH3_0$)		**CH2** ($CH2_1$ $CH2_0$)		**CH1** ($CH1_1$ $CH1_0$)	
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
CHn	2n-2 :2n-1	r	**Standard Diagnosis for Channel n** 00 Short circuit to ground 01 Open load 10 Over load / over temperature 11 Normal operation

6.1 SPI Examples

Below are examples of the different SPI command words and the resulting behavior of the output channels and Seiral Output pin.

6.1.1 Example: Diagnosis Only

The contents of the diagnosis register will be returned during the next SPI access. This command is only active once unless the next control command is again “Diagnosis only” (see **Figure 14**).

In the example shown in **Figure 14**, the standard diagnosis reports short circuit to ground for channel 1 (00), open load for channel 2 (01), over load / over temperature for channel 3 (10) and normal operation for channel 4 (11).

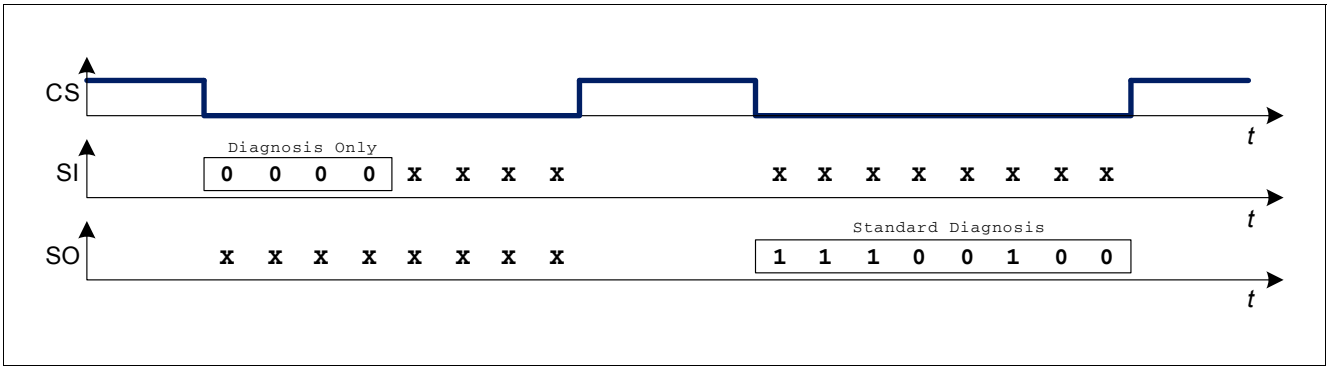


Figure 14 Diagnosis Only

6.1.2 Example: Read Back Input and 1-bit Diagnosis

The first four bits of SO during the next SPI access give the state of the parallel inputs, denoted by *INn*. The second four-bit word fed out at SO contains 1-bit diagnosis information of the output (1 = no fault, 0 = fault), denoted by *Fn* (see **Figure 15**).

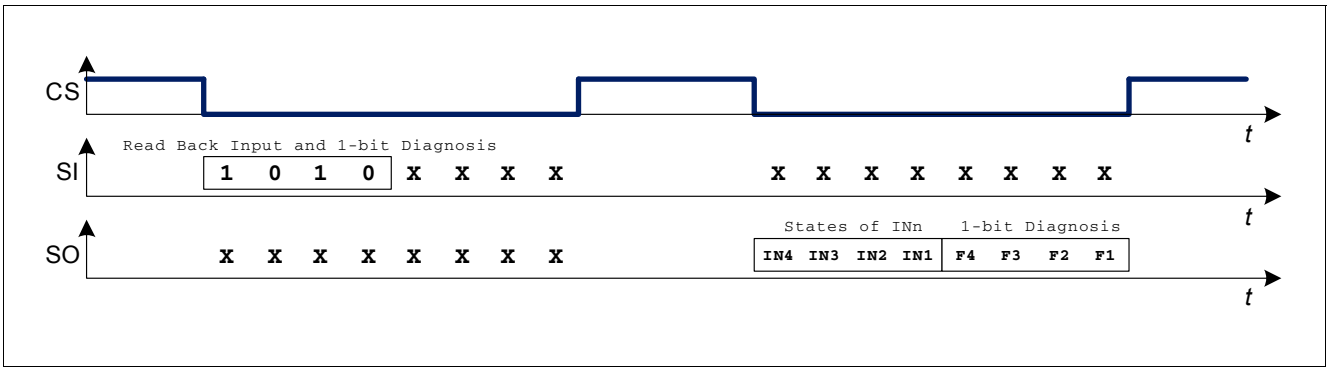


Figure 15 Read Back Input and 1-bit Diagnosis

6.1.3 Example: Echo Function of SPI

This function can be used to check the proper function of the serial interface. This command connects directly the SI to the SO during the next CS period. This internal connection is only active once unless the next control command is again “Echo function of SPI” (see **Figure 16**).

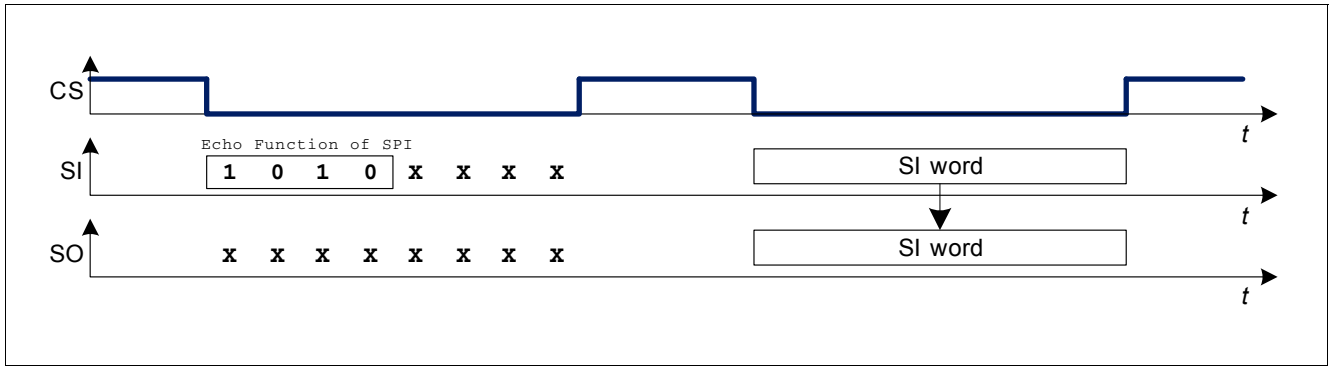


Figure 16 Echo Function of SPI

6.1.4 Example: OR Operation and Diagnosis

Sets the *BOL* bit to perform an OR operation on the *INn* signals and their corresponding data bits CHn_{IN}. The contents of the diagnosis register will be returned during the next SPI access (see **Figure 17**). If the OR operation is programmed, it is latched until overwritten by an AND operation. This is the default operation after the device emerges from power-up or Reset mode.

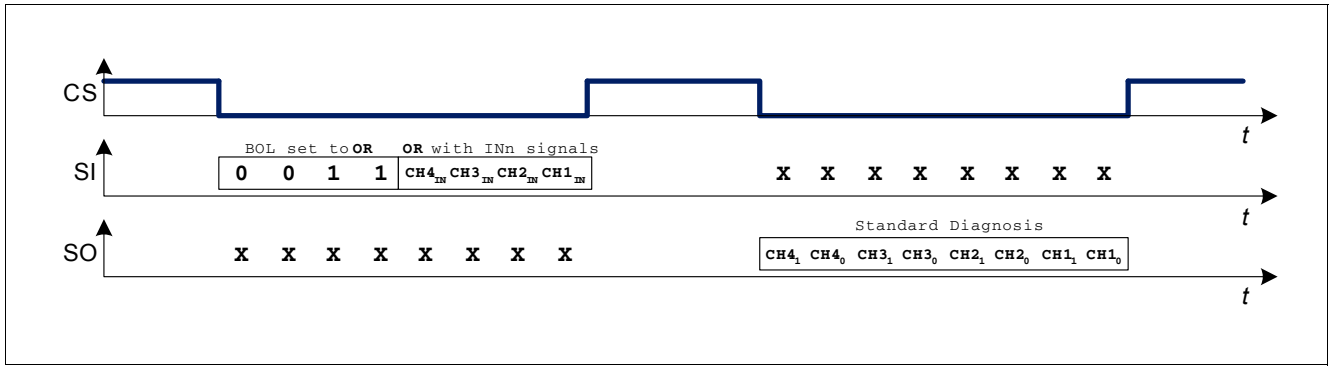


Figure 17 OR Operation and Diagnosis

6.1.5 Example: AND Operation and Diagnosis

Sets the *BOL* bit to perform an AND operation on the *INn* signals and their corresponding data bits CHn_{IN}. The contents of the diagnosis register will be returned during the next SPI access (see **Figure 18**). If the AND operation is programmed, it is latched until overwritten by an OR operation, the device enters Reset mode or becomes shut down.

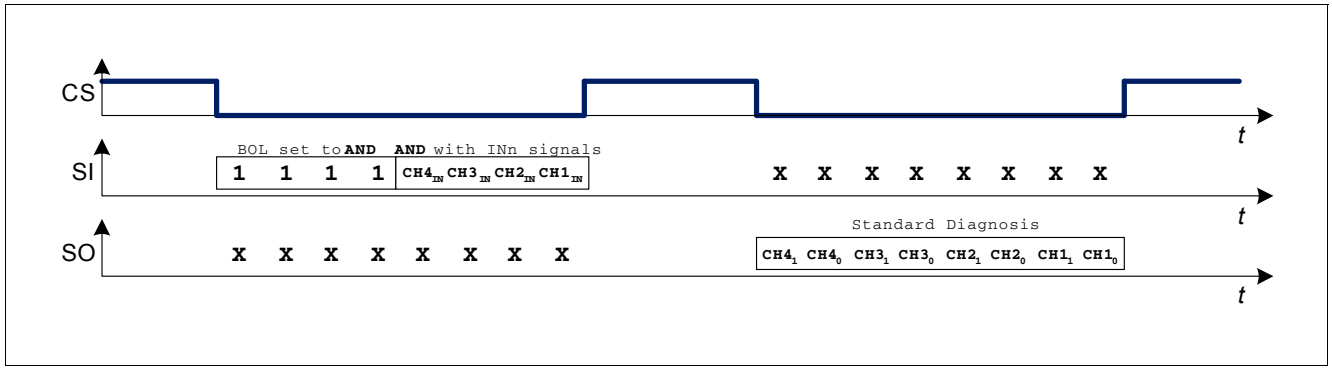


Figure 18 AND Operation and Diagnosis

6.1.6 Example: All Other Command Words

All other control words except for Diagnosis Only, Read Back Input and Echo Function will be accepted as an OR or an AND command with valid data bits, depending on the Boolean operation which was previously programmed (see **Figure 19**).

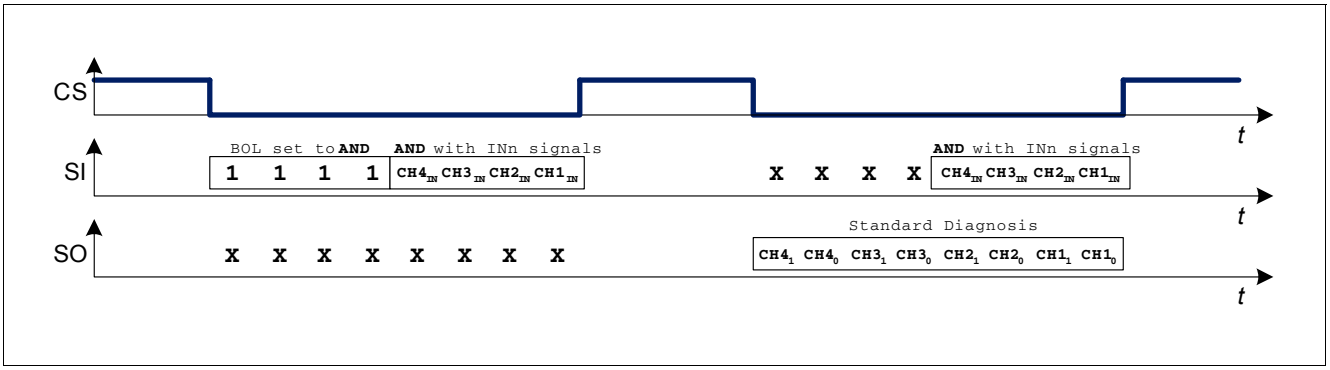


Figure 19 All Other Command Words (with previously programmed AND command)

7 Application Description

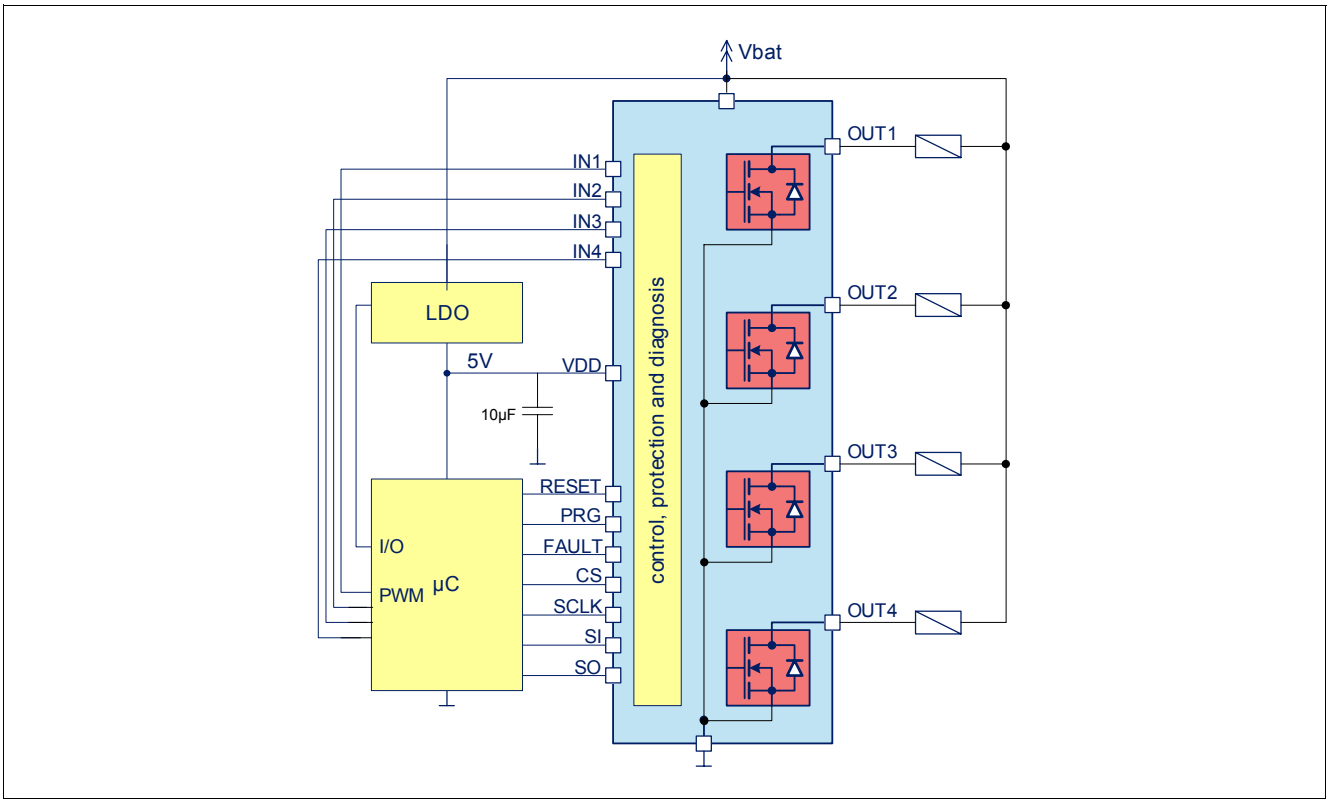
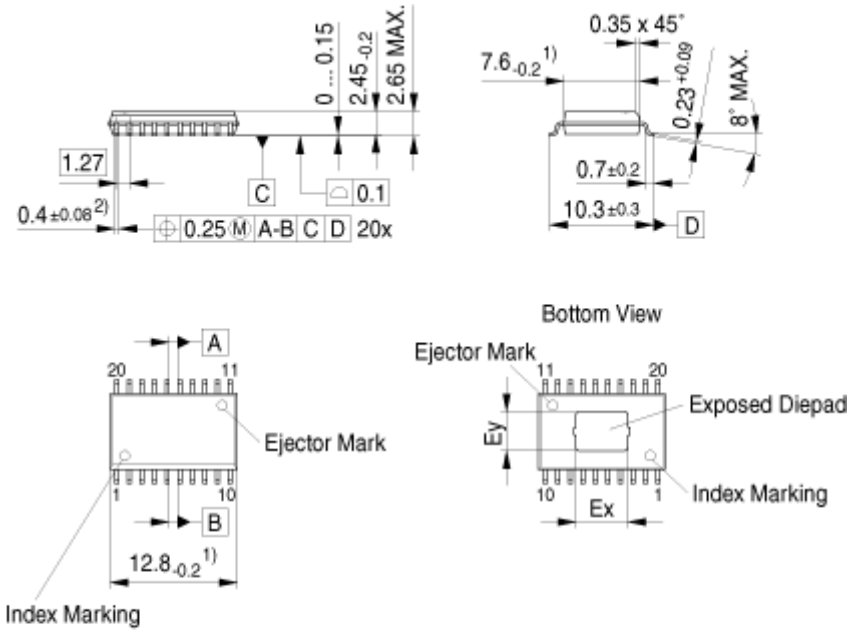


Figure 20 Application Circuit

8 Package Outlines



Exposed Diepad Dimensions			
Leadframe	Leadframe	Ex	Ey
PG-DSO-20-27	C66065-A6680-C005	5.2	4.6
PG-DSO-20-30	C66065-A6680-C009	7	4.8
PG-DSO-20-38	C66065-A6680-C003	7	4.8

1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion of 0.05 max. per side

GPS01059

Figure 21 PG-DSO-20-30 (Plastic Dual Small Outline Package) Green Product

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: **http://www.infineon.com/products**.

Dimensions in mm

9 Revision History

Version	Date	Changes
V1.0 -> V1.1: 2008-03-02		
V1.1	2008-03-03	typo corrected page 3: from “Description / Quad Current Sense Low-Side Switch in Smart Power Technology (SPT) with four open drain DMOS output stages....” to “Description / Quad Low-Side Switch in Smart Power Technology (SPT) with four open drain DMOS output stages. ...
V0.5 -> V1.0: 2007-06-11 Version Change to “Final” Data Sheet		
V1.0	2007-06-11	Information under Maximum Ratings about “DIN Humidity Category” and “IEC Climatic Category” according data sheet standards removed.
V1.0	2007-07-10	Thermal Information Chapter 4.2 added
V1.0	2007-07-26	Fig 21 updated

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