

Document Title**512Kx16 bit Low Power Full CMOS Static RAM****Revision History**

<u>Revision No.</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
0.0	Initial draft	October 31, 2002	Preliminary
0.1	Revised - Deleted 44-TSOP2-400R package type.	December 11, 2002	Preliminary
1.0	Finalized - Changed Icc1 from 4mA to 3mA - Changed Icc2 from 45mA to 30mA - Changed ISB1(industrial) from 30mA to 15mA - Changed ISB1(Automotive) from 40mA to 25mA	September 16, 2003	Final

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512Kx16 bit Low Power Full CMOS Static RAM

FEATURES

- Process Technology: Full CMOS
- Organization: 512K x16
- Power Supply Voltage: 2.7~3.6V
- Low Data Retention Voltage: 1.5V(Min)
- Three state outputs
- Package Type: 44-TSOP2-400F

GENERAL DESCRIPTION

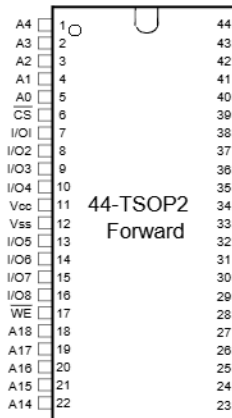
The K6X8016T3B families are fabricated by SAMSUNG's advanced full CMOS process technology. The families support various operating temperature range for user flexibility of system design. The families also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation		PKG Type
				Standby (Isb1, Max)	Operating (Icc2, Max)	
K6X8016T3B-F	Industrial(-40~85°C)	2.7~3.6V	55 ¹⁾ /70ns	15 μ A	30mA	44-TSOP2-400F
K6X8016T3B-Q	Automotive(-40~125°C)		70ns	25 μ A		

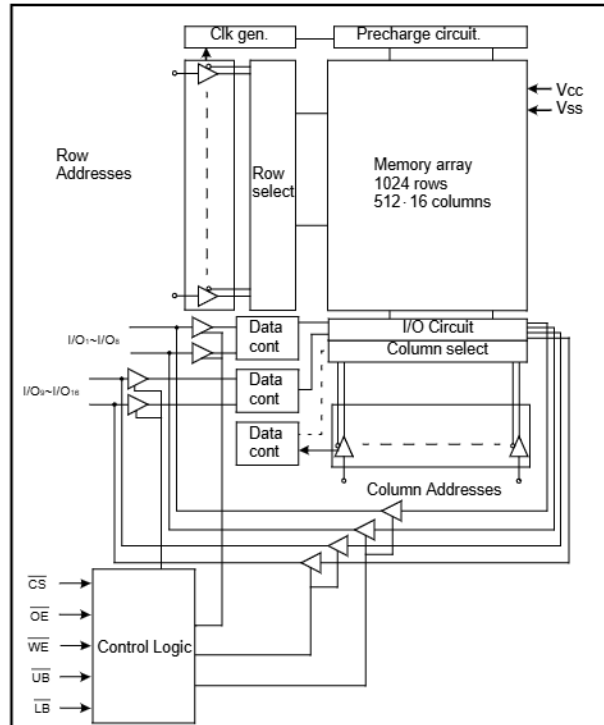
1. This parameter is measured with 50pF test load (Vcc=3.0~3.6V).

PIN DESCRIPTION



Name	Function	Name	Function
$\overline{CS}$	Chip Select Input	Vcc	Power
$\overline{OE}$	Output Enable Input	Vss	Ground
$\overline{WE}$	Write Enable Input	$\overline{UB}$	Upper Byte(I/O9~16)
A0~A18	Address Inputs	$\overline{LB}$	Lower Byte(I/O1~8)
I/O1~I/O16	Data Inputs/Outputs		

FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONICS CO., LTD. reserves the right to change products and specifications without notice.

PRODUCT LIST

Industrial Temperature Products(-40~85°C)		Automotive Temperature Products(-40~125°C)	
Part Name	Function	Part Name	Function
K6X8016T3B-TF55 ¹⁾	44-TSOP2-F, 55ns, Low Low Power	K6X8016T3B-TQ70	44-TSOP2-F, 70ns, Low Power
K6X8016T3B-TF70	44-TSOP2-F, 70ns, Low Low Power		

1. Operating voltage range is 3.0~3.6V

FUNCTIONAL DESCRIPTION

$\overline{\text{CS}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	$\overline{\text{LB}}$	$\overline{\text{UB}}$	I/O1~8	I/O9~16	Mode	Power
H	X	X	X	X	High-Z	High-Z	Deselected	Standby
L	H	H	X	X	High-Z	High-Z	Output Disabled	Active
L	X	X	H	H	High-Z	High-Z	Output Disabled	Active
L	L	H	L	H	Dout	High-Z	Lower Byte Read	Active
L	L	H	H	L	High-Z	Dout	Upper Byte Read	Active
L	L	H	L	L	Dout	Dout	Word Read	Active
L	X	L	L	H	Din	High-Z	Lower Byte Write	Active
L	X	L	H	L	High-Z	Din	Upper Byte Write	Active
L	X	L	L	L	Din	Din	Word Write	Active

Note: X means don't care. (Must be low or high state)

ABSOLUTE MAXIMUM RATINGS¹⁾

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-0.2 to V _{CC} +0.3 (max. 3.9V)	V	-
Voltage on Vcc supply relative to	V _{CC}	-0.2 to 3.9	V	-
Power Dissipation	P _D	1.0	W	-
Storage temperature	T _{STG}	-65 to 150	°C	-
Operating Temperature	T _A	-40 to 85	°C	K6X8016T3B-F
		-40 to 125	°C	K6X8016T3B-Q

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS¹⁾

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V _{CC}	2.7	3.0/3.3	3.6	V
Ground	V _{SS}	0	0	0	V
Input high voltage	V _{IH}	2.2	-	V _{CC} +0.3 ²⁾	V
Input low voltage	V _{IL}	-0.3 ³⁾	-	0.6	V

Note:

1. Industrial Product: T_A=-40 to 85°C, otherwise specified.
Automotive Product: T_A=-40 to 125°C, otherwise specified.
2. Overshoot: V_{CC}+3.0V in case of pulse width ≤30ns.
3. Undershoot: -3.0V in case of pulse width ≤30ns.
4. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE¹⁾ (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C _{IN}	V _{IN} =0V	-	8	pF
Input/Output capacitance	C _{IO}	V _{IO} =0V	-	10	pF

1. Capacitance is sampled, not 100% tested

DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions	Min	Typ	Max	Unit	
Input leakage current	I _{LI}	V _{IN} =V _{ss} to V _{cc}	-1	-	1	αA	
Output leakage current	I _{LO}	$\overline{CS}$ =V _{IH} , $\overline{OE}$ =V _{IH} or $\overline{WE}$ =V _{IL} , V _{IO} =V _{ss} to V _{cc}	-1	-	1	αA	
Operating power supply current	I _{CC}	I _{IO} =0mA, $\overline{CS}$ =V _{IL} , $\overline{WE}$ =V _{IH} , V _{IN} =V _{IH} or V _{IL}	-	-	2	mA	
Average operating current	I _{CC1}	Cycle time=1αs, 100% duty, I _{IO} =0mA, $\overline{CS}$ ≤0.2V, V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	-	-	3	mA	
	I _{CC2}	Cycle time=Min, I _{IO} =0mA, 100% duty, $\overline{CS}$ =V _{IL} , V _{IN} =V _{IL} or V _{IH}	-	-	30	mA	
Output low voltage	V _{OL}	I _{OL} = 2.1mA	-	-	0.4	V	
Output high voltage	V _{OH}	I _{OH} = -1.0mA	2.4	-	-	V	
Standby Current(TTL)	I _{SB}	$\overline{CS}$ =V _{IH} , Other inputs=V _{IH} or V _{IL}	-	-	0.4	mA	
Standby Current(CMOS)	I _{SB1}	$\overline{CS}$ ≥V _{CC} -0.2V, Other inputs=0~V _{CC}	K6X8016T3B-F	-	-	15	αA
			K6X8016T3B-Q	-	-	25	

AC OPERATING CONDITIONS

TEST CONDITIONS (Test Load and Input/Output Reference)

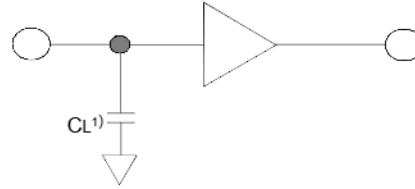
Input pulse level: 0.4 to 2.2V

Input rising and falling time: 5ns

Input and output reference voltage: 1.5V

Output load(see right): $C_L = 100\text{pF} + 1\text{TTL}$

$C_L = 50\text{pF} + 1\text{TTL}$



1. Including scope and jig capacitance

AC CHARACTERISTICS ($V_{CC} = 2.7 \sim 3.6\text{V}$, Industrial product: $T_A = -40$ to 85°C , Automotive product: $T_A = -40$ to 125°C)

Parameter List		Symbol	Speed Bins				Units
			55ns ¹⁾		70ns		
			Min	Max	Min	Max	
Read	Read cycle time	tRC	55	-	70	-	ns
	Address access time	tAA	-	55	-	70	ns
	Chip select to output	tCO	-	55	-	70	ns
	Output enable to valid output	tOE	-	25	-	35	ns
	Chip select to low-Z output	tLZ	10	-	10	-	ns
	Output enable to low-Z output	tOLZ	5	-	5	-	ns
	$\overline{\text{LB}}$, $\overline{\text{UB}}$ enable to low-Z output	tBLZ	5	-	5	-	ns
	Chip disable to high-Z output	tHZ	0	20	0	25	ns
	Output Disable to High-Z Output	tOHZ	0	20	0	25	ns
	Output hold from address change	tOH	10	-	10	-	ns
	$\overline{\text{LB}}$, $\overline{\text{UB}}$ valid to data output	tBA	-	25	-	35	ns
	$\overline{\text{UB}}$, $\overline{\text{LB}}$ disable to high-Z output	tBHZ	0	20	0	25	ns
Write	Write cycle time	tWC	55	-	70	-	ns
	Chip select to end of write	tCW	45	-	60	-	ns
	Address set-up time	tAS	0	-	0	-	ns
	Address valid to end of write	tAW	45	-	60	-	ns
	Write pulse width	tWP	40	-	55	-	ns
	Write recovery time	tWR	0	-	0	-	ns
	Write to output high-Z	tWHZ	0	20	0	25	ns
	Data to write time overlap	tDW	20	-	30	-	ns
	Data hold from write time	tDH	0	-	0	-	ns
	End write to output low-Z	tOW	5	-	5	-	ns
	$\overline{\text{LB}}$, $\overline{\text{UB}}$ valid to end of write	tBW	45	-	60	-	ns

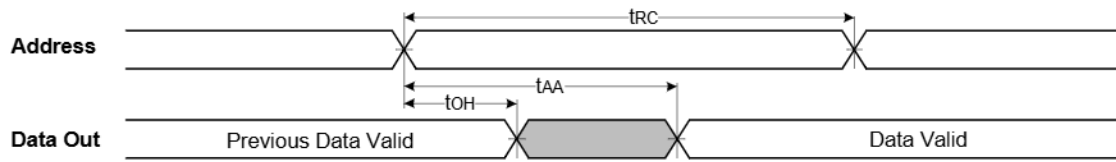
1. Voltage range is 3.0V~3.6V for industrial product.

DATA RETENTION CHARACTERISTICS

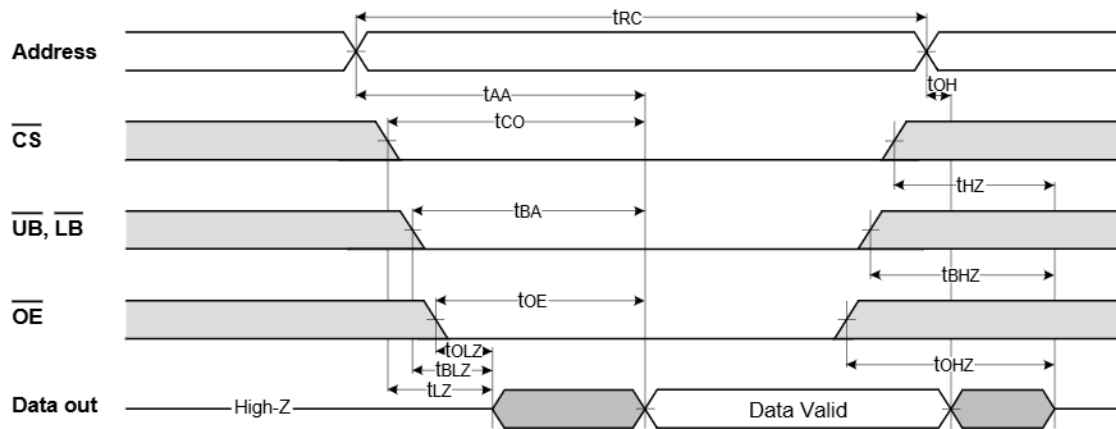
Item	Symbol	Test Condition	Min	Typ	Max	Unit
V _{CC} for data retention	V _{DR}	$\overline{\text{CS}} \geq V_{CC} - 0.2\text{V}$	1.5	-	3.6	V
Data retention current	I _{DR}	$V_{CC} = 1.5\text{V}$, $\overline{\text{CS}} \geq V_{CC} - 0.2\text{V}$	K6X8016T3B-F	-	6	μA
			K6X8016T3B-Q	-	10	
Data retention set-up time	t _{SDR}	See data retention waveform	0	-	-	ms
Recovery time	t _{RDR}		5	-	-	

TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}=\overline{OE}=V_{IL}$, $\overline{WE}=V_{IH}$, $\overline{UB}$ or/and $\overline{LB}=V_{IL}$)



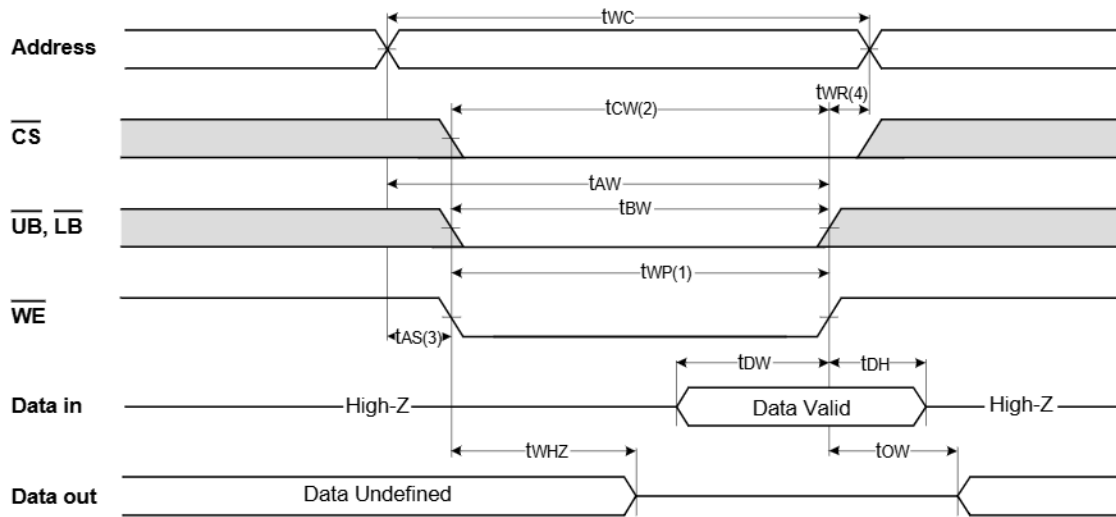
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}=V_{IH}$)



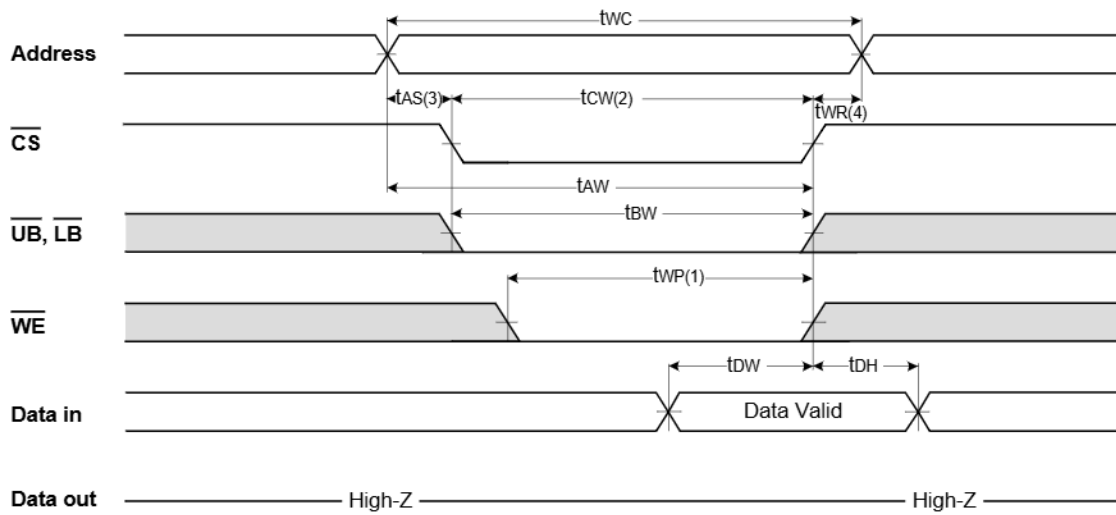
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, $t_{HZ}(\text{Max.})$ is less than $t_{LZ}(\text{Min.})$ both for a given device and from device to device interconnection.

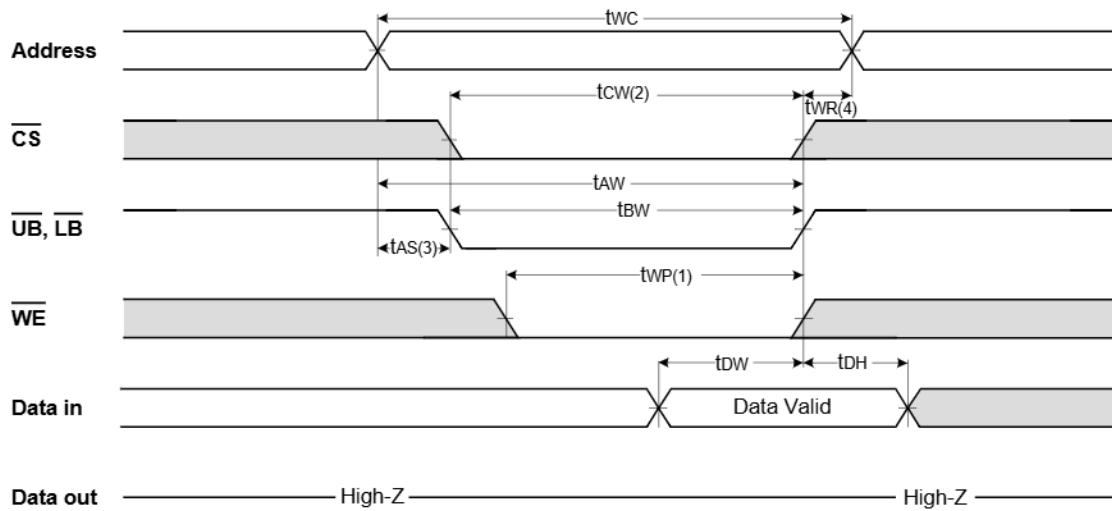
TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) ($\overline{UB}$, $\overline{LB}$ Controlled)

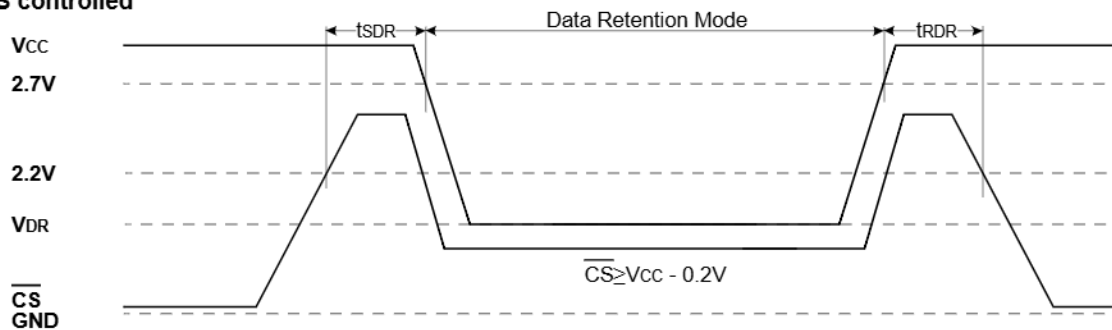


NOTES (WRITE CYCLE)

1. A write occurs during the overlap(t_{WP}) of low $\overline{CS}$ and low $\overline{WE}$. A write begins when $\overline{CS}$ goes low and $\overline{WE}$ goes low with asserting $\overline{UB}$ or $\overline{LB}$ for single byte operation or simultaneously asserting $\overline{UB}$ and $\overline{LB}$ for double byte operation. A write ends at the earliest transition when $\overline{CS}$ goes high and $\overline{WE}$ goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{CS}$ going low to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.

DATA RETENTION WAVE FORM

$\overline{CS}$ controlled



PACKAGE DIMENSIONS

Unit: millimeters(inches)

44 PIN THIN SMALL OUTLINE PACKAGE TYPE II (400F)

