N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope and designed for use as a line interrupter in telephone sets and for application in relay, high-speed and line-transformer drivers.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching.
- No secondary breakdown.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	250	V
Drain current (DC)	I_D	max.	350	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1.5	W
Drain-source on-resistance I_D = 300 mA; V_{GS} = 10 V	$R_{DS(on)}$	typ.	5.0	Ω
		max.	7.0	Ω
Gate-source threshold voltage	$V_{GS(th)}$	max.	2	V

MECHANICAL DATA

Dimensions in mm

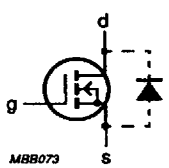
Marking code

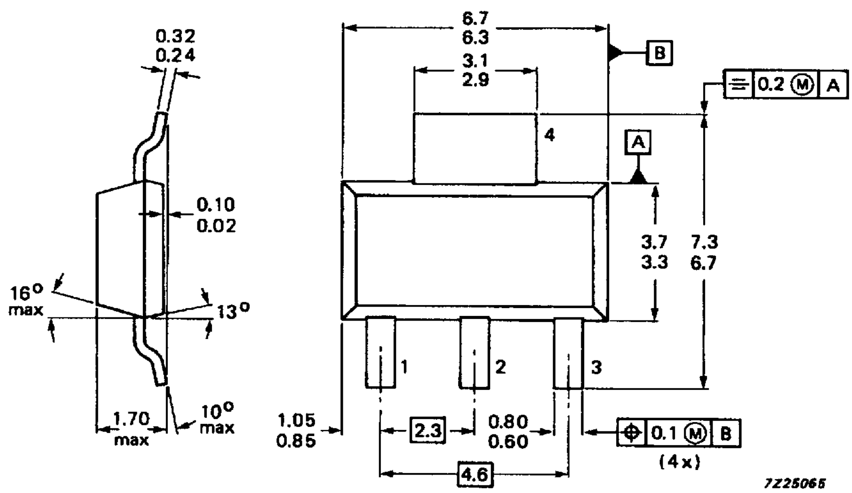
BSP126

Fig.1 SOT223.

Pinning

1 = gate
2 = drain
3 = source
4 = drain





RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	250	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	350	mA
Drain current (peak)	I_{DM}	max.	1.2	A
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1.5	W
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	83.3	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 10 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	250	V
Drain-source leakage current V_{DS} = 200 V; V_{GS} = 0	I_{DSS}	max.	1.0	μA
Gate-source leakage current $\pm V_{GS}$ = 20 V; V_{DS} = 0	$\pm I_{GSS}$	max.	100	nA
Gate threshold voltage I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min. max.	0.8 2.0	V V
Drain-source on-resistance I_D = 300 mA; V_{GS} = 10 V	$R_{DS(on)}$	typ. max.	5.0 7.0	Ω Ω
I_D = 20 mA; V_{GS} = 2.4 V	$R_{DS(on)}$	max.	10	Ω
Transfer admittance I_D = 300 mA; V_{DS} = 25 V	$\|Y_{fs}\|$	min. typ.	200 400	mS mS
Input capacitance at f = 1 MHz; V_{DS} = 25 V; V_{GS} = 0	C_{iss}	typ. max.	65 90	pF pF
Output capacitance at f = 1 MHz; V_{DS} = 25 V; V_{GS} = 0	C_{oss}	typ. max.	20 30	pF pF
Feedback capacitance at f = 1 MHz; V_{DS} = 25 V; V_{GS} = 0	C_{rss}	typ. max.	5 15	pF pF

Note

1. Device mounted on an epoxy printed-circuit board 40 mm x 40 mm x 1.5 mm; mounting pad for the drain lead min. 6 cm^2.

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Switching times (see Figs 2 and 3)			
I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V			
t_{on}	typ.	5	ns
	max.	10	ns
t_{off}	typ.	20	ns
	max.	30	ns

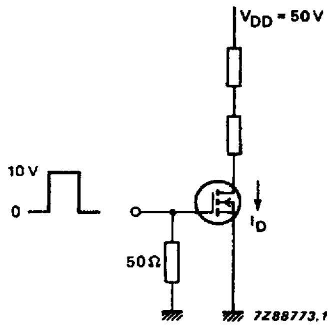

Fig.2 Switching time test circuit.

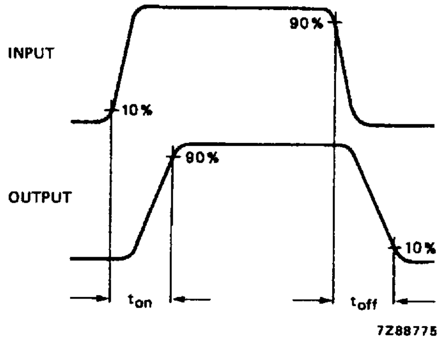

Fig.3 Input and output waveforms.

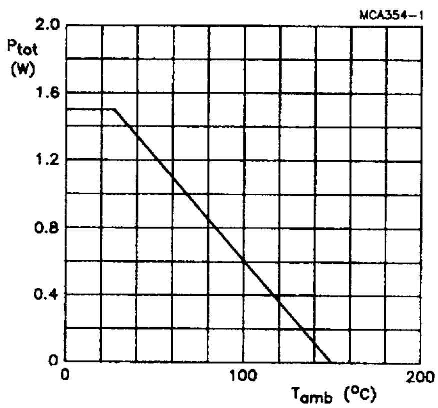

Fig.4 Power derating curve.

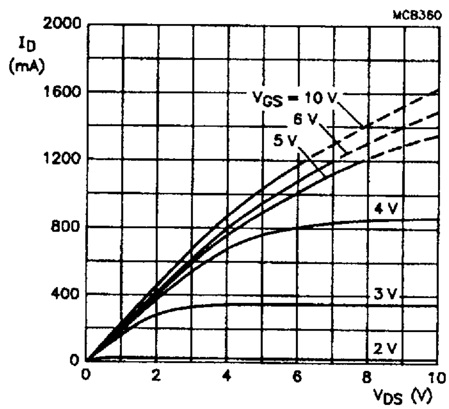

Fig.5 Output characteristics; T_j = 25 °C; typical values.

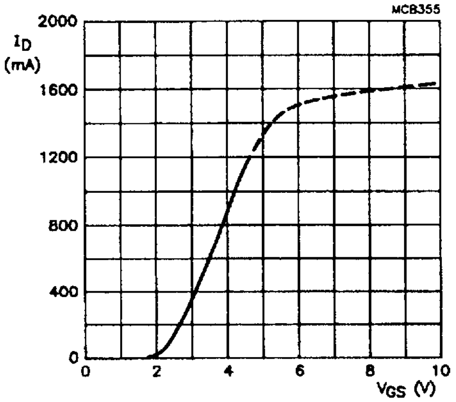

Fig.6 Transfer characteristic; V_{DS} = 10 V; T_j = 25 °C; typical value.

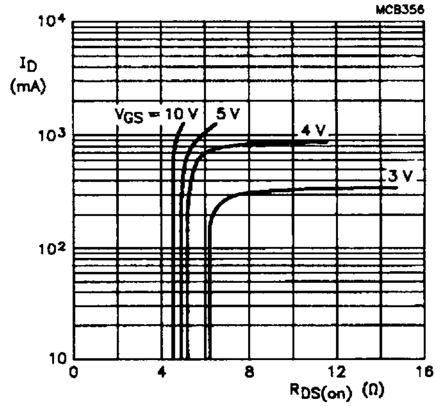

Fig.7 On-resistance as a function of drain current; T_j = 25 °C; typical values.

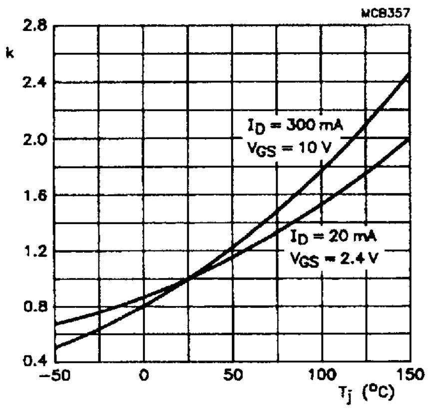

Fig.8 $k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ ^\circ C}$; typical values.

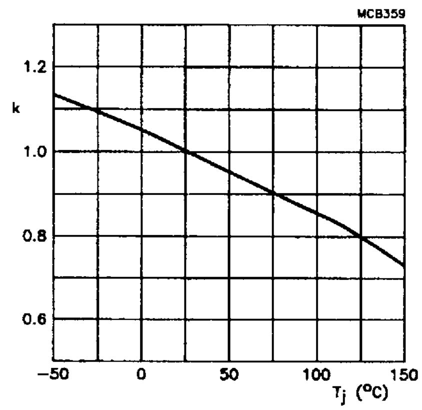

Fig.9 $k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ ^\circ C}$; $V_{GS(th)}$ at 1 mA; typical values.

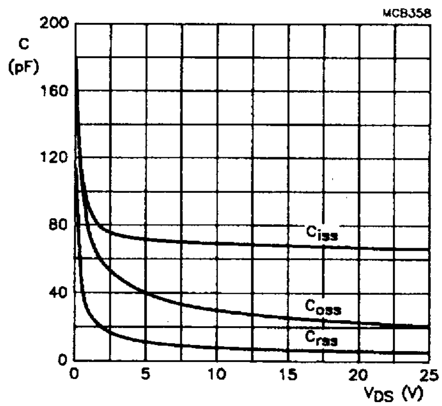

Fig.10 Capacitances as a function of drain-source voltage; $V_{GS} = 0$; f = 1 MHz; $T_j = 25\ ^oC$; typical values.